

## Eaton capacitors dielectric performance under dc voltage stress

A utility in the Southwest reported repeated failures of capacitors at one of their ungrounded-wye banks. The failures were noticed upon bank energization after the bank had been disconnected as a result of a normal switching operation.

After repeated failures, the utility installed replacement capacitors from a second manufacturer and still had similar failures. After experiencing the same failures, they attached monitoring equipment to the bank and discovered that the failures occurred shortly after de-energization, not upon energization as originally thought.

Eaton analyzed the circumstances and the investigation concluded that the cause of the failure was the dc withstand of all-film capacitors and how the higher dc levels present after de-energizing a capacitor bank compared with the dc withstand. The findings are also compounded by the fact that high temperature plays a role in the dc performance of the capacitor dielectric system. This, coupled with the higher dc voltages trapped in ungrounded-wye capacitor banks, was the root cause for the failures experienced by the utility. Given the field experience by this utility with capacitors from various manufacturers, Eaton concluded that this was most likely an industry-wide concern.

The following factors were determined to be critical in how these failures occurred:

1. Capacitors are under dc voltage stress upon de-energization as the discharge resistor removes the stored charge.
2. Capacitor dc voltage stress withstand is reduced over time.
3. The dc voltage stress withstand is further reduced at high-operating temperatures.
4. The dielectric fluid properties and the pad thickness (the thickness of polypropylene between two conducting foils in the capacitor winding) have a significant impact on the dc stress withstand performance of capacitors.

### dc voltage stress

Capacitors operate under ac voltage at power system frequency when energized. Once disconnected from the power system, capacitors are exposed to dc voltage until the trapped charge is totally dissipated by the required discharge resistor connected between the capacitor terminals. The magnitude of this trapped dc voltage depends on the capacitor bank configuration—grounded-wye or ungrounded-wye.

### Grounded-wye capacitor banks

De-energizing a capacitor bank always results in a trapped dc voltage in the capacitor as the current interruption always occurs at a current zero and, given the 90-degree phase angle relationship between voltage and current through a capacitor, the trapped voltage is always at peak value. The trapped dc voltage upon de-energization of a grounded-wye capacitor bank is the peak value of the system line-to-ground rms voltage or  $\sqrt{2} \times V_{\text{sys}}$  (that is, 1 pu).

**Figure 1** shows the current and voltage oscillograms upon de-energization of a grounded-wye capacitor bank. The trip command is shown as the dashed, red vertical line. The current traces show how each phase current is interrupted at the first zero current crossing immediately after the trip command. This occurs even with gang-operated switching devices. The trapped voltage for each phase is shown as a positive or negative peak value (1 pu) at the time the corresponding phase current is interrupted.



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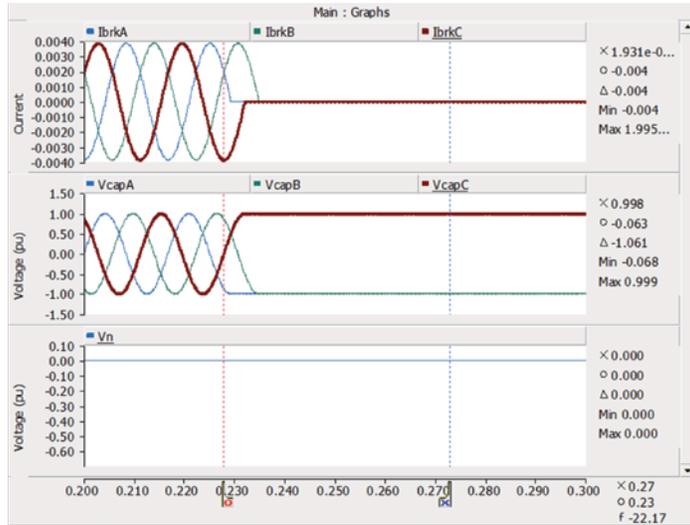


Figure 1. Current and voltage traces during de-energization of a grounded-wye capacitor bank

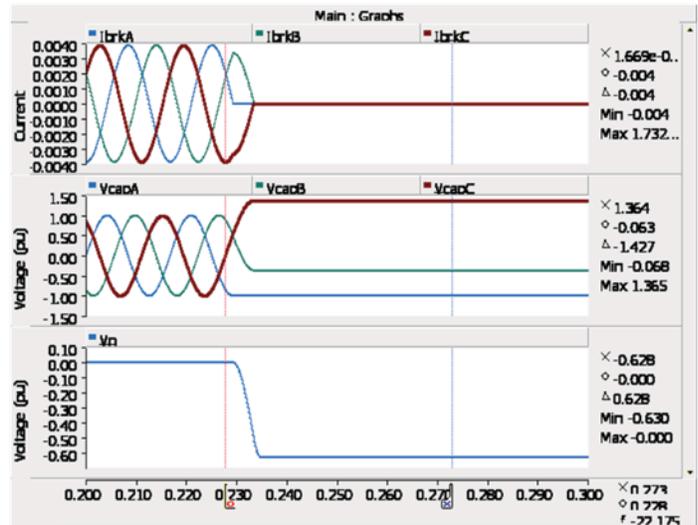


Figure 2. Current and voltage traces during de-energization of an ungrounded-wye capacitor bank

### Ungrounded-wye capacitor banks

The trapped dc voltage upon de-energization of an ungrounded-wye capacitor bank depends on the neutral voltage at the time of interruption. The trapped voltage in the capacitor on the first phase to interrupt the current is + or - 1 pu. The magnitudes of the trapped voltages on the capacitors on the other two phases depend on when their current is interrupted. It can be much higher than 1 pu.

Figure 2 shows the current and voltage oscillograms upon de-energization of an ungrounded-wye capacitor bank. Again, the trip command is shown as the dashed, red vertical line. The phase currents are interrupted at the first zero current crossing immediately after the trip command with phase A being the first to be interrupted. At the next current zero, both B and C phase currents are interrupted as the capacitors in these two phases are now connected in series with line-to-line voltage applied across the two capacitors (Figure 3). The bottom trace shows the neutral voltage and how it shifts with respect to ground after the phase A current is interrupted, causing the voltage on the phase C capacitor to reach a peak value of 1.36 pu at the time its current is interrupted. This is the trapped dc voltage level on this capacitor and will decay slowly due to the discharge resistor connected between the capacitor terminals.

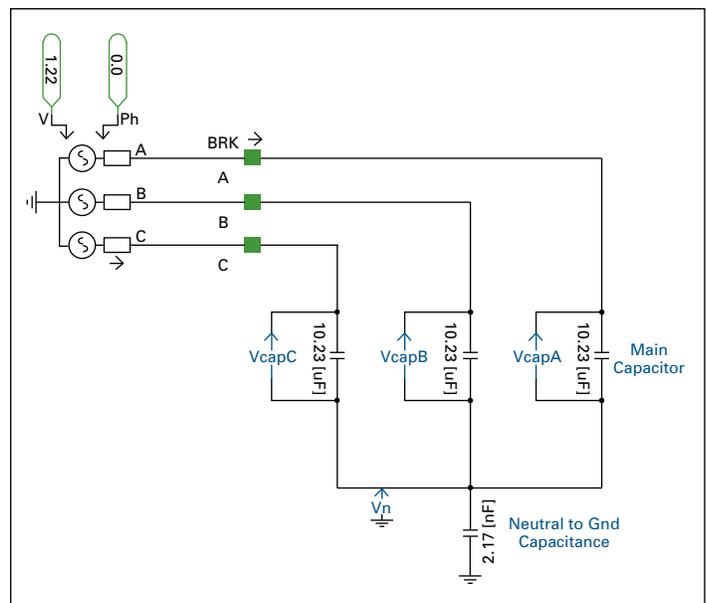


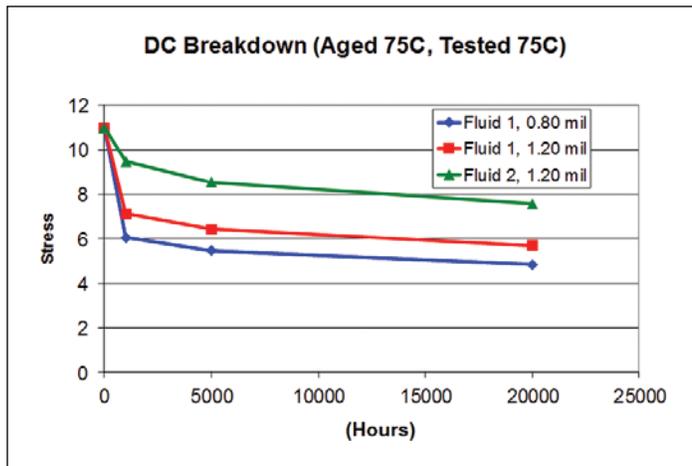
Figure 3. Ungrounded-wye capacitor bank schematic circuit

## Capacitor dc voltage stress withstand

The performance of an all-film capacitor under ac voltage is affected by the dielectric material characteristics, temperature, and the pad thickness. The ac performance of the dielectric is relatively constant during the expected life of the capacitor with a thicker pad more susceptible to failure under ac voltage stress than a thinner pad at similar operating stress levels.

An all-film capacitor performance under dc voltage is affected by the dielectric material characteristics, temperature, and the pad thickness. The dc performance of the dielectric decreases very rapidly after first 40 to 50 days of energization at system voltage and then remains relatively constant during the expected life of the capacitor. Also, a thinner pad is more susceptible to failure under dc voltage stress than a thicker pad under similar electrical stress and temperature.

**Figure 4** shows how the dc withstand of all-film capacitors and how the dc withstand level is significantly reduced during the first 1000 hours of operation at system voltage. The figure also shows how the dc stress withstand is impacted by the properties of the dielectric fluid and the dielectric pad thickness. The dc voltage stress withstand is further reduced at high-operating temperatures.



**Figure 4. dc stress withstand of an all-film capacitor dielectric system**

## Eaton’s design and routine tests approach

As a result of the investigation, Eaton formulated a dielectric fluid with superior high-temperature dc and discharge inception voltage (DIV) performance, the Edisol® VI dielectric fluid, and uses it on all capacitor units they manufacture. In addition, the design rules were modified to limit the minimum thickness of the dielectric system used in Eaton’s capacitors. The dc performance of the Eaton design with the Edisol VI dielectric fluid is shown in **Figure 4** (Fluid 2, green graph).

In addition to the new dielectric fluid formulation and design rule changes, Eaton implemented changes to the ac routine test regimen, above what is required by the capacitor standards. IEEE® Std 18 states that either one of these tests be performed on all capacitor units:

- 2x rated voltage ac test
- 4.3x rated voltage dc test

The objective was to establish factory tests that can predict both the ac and dc long-term performance in the field for our capacitor units. As a result, Eaton always performs a dc test on all capacitors to ensure that the field-conditioned capacitors’ dc withstand remains above the trapped dc voltage level following de-energization, even if the customer’s specifications opt for the ac tests only as allowed by the standards. The level of the dc voltage applied for this test was determined considering the following:

- Trapped dc voltage in the capacitor under worst conditions (ungrounded-wye capacitor bank configuration)
- Reduction in dc stress withstand within days of being energized at system voltage
- Reduction in dc stress withstand in high-ambient temperature environments

Eaton’s routine test for standard duty (SD) and heavy duty (HD) capacitor types includes both 2x rated ac test and 3.25x rated dc if the customer specifies the ac test. If the dc test is specified, then Eaton performs it in accordance with the standards at 4.3x rated dc.

Eaton’s routine tests exceed the requirements of IEEE Std 18 to assess the capacitor capability to perform at the reduced dc withstand (after conditioning) in ungrounded capacitor banks operating in high-temperature environments.

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