Time current curves Power Defense MCCB
Frame 4 thermal-magnetic and PXR electronic trip units
Standards: UL, CSA, IEC, CCC

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## Table 1. Revision notes

*Note:* Unless noted below, all curves remain unchanged from their prior revision.

<table>
<thead>
<tr>
<th>Revision</th>
<th>Curve number</th>
<th>Page</th>
<th>Date</th>
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<td>Power Defense frame 4 initial release</td>
<td></td>
<td></td>
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<tr>
<td>2</td>
<td></td>
<td></td>
<td>11/2019</td>
</tr>
<tr>
<td></td>
<td>Short delay tolerances adjusted for phase and ground on I/t slopes.</td>
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This information is provided only as an aid to understand the catalog numbers. It is not to be used to build catalog numbers for circuit breakers or trip units as all combinations may not be available.

Table 2. Catalog number convention

<table>
<thead>
<tr>
<th>Breaker family</th>
<th>Trip unit type</th>
<th>Terminals included</th>
</tr>
</thead>
<tbody>
<tr>
<td>PDG4 = Frame 4 global UL / CSA / IEC / GB</td>
<td>TI# = Thermal magnetic trip unit (1)</td>
<td>N = No terminals</td>
</tr>
<tr>
<td>PDG4 = Frame 4 global-100% UL / CSA / IEC / GB (uses PDG trip units)</td>
<td>V## = 50°C calibrated thermal magnetic trip unit (1)</td>
<td>J = Line and load terminals</td>
</tr>
<tr>
<td>PDC4 = Frame 4 IEC / GB</td>
<td>B## = PXR 10 (1)</td>
<td>K = Line only terminals</td>
</tr>
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</table>

Note: 1 See catalog for ### (protection type and available configured options).

Table 3. Electronic trip unit catalog number convention

<table>
<thead>
<tr>
<th>Style family</th>
<th>Trip unit</th>
<th>Features</th>
</tr>
</thead>
<tbody>
<tr>
<td>PDG4 = Frame 4 global UL / CSA / IEC / GB for PDG and PDF breakers</td>
<td>PXR = Electronic trip unit</td>
<td>N = None</td>
</tr>
<tr>
<td>PDC4 = Frame 4 IEC / GB for PDC and PDF breakers</td>
<td>PXR = Electronic trip unit</td>
<td>R = Relays</td>
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</table>

Note: IEC standard breakers include the CE mark; GB standard breakers include the CCC mark.
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Frame 4 thermal-magnetic and PXR electronic trip units
Standards: UL, CSA, IEC, CCC

Table 4. Magnetic trip unit thermal catalog number convention

Table 5. Symmetrical RMS interruption ratings (kA) for each breaker frame

Table 6. Curve notes

1. These curves apply for 50Hz and 60Hz applications.
2. The maximum voltage rating for the frame style is stated in Table 5.
3. These curves are comprehensive for Power Defense style circuit breakers including frame sizes, ratings and constructions stated.
4. The total clearing times shown include the response time for the trip unit, the breaker opening and the interruption of the current. The bottom of the time band is the minimum commit to trip time.
5. The end of the curve is determined by the application or the interrupting rating of the circuit breaker.
6. Thermal magnetic trip unit calibration based on 40°C ambient, cold start. Tested with 4 feet of rated wire (75°C) per terminal. Tested in open air with current in all poles.
7. Thermal magnetic trip unit instantaneous calibration based on single pole testing.
8. All electronic trip units have an over temperature protection feature that will trip the breaker when the internal temperature of the ETU is over 105°C.
9. All time current data for PXR is based on 3 phase testing.

Note: IEC standard breakers include the CE mark; GB standard breakers include the CCC mark.

*800A frame unless noted
Figure 1. Power Defense frame 4 trip unit front labels

Note: Trip unit drawings in Figure 1 are representative of the face plates provided. Values on the trip unit dials will change based upon the specific breaker and trip unit. Refer to the time current curve of the breaker or the PXR User Guide for the specific settings.
Time current curves Power Defense MCCB
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Curves

Figure 2. PXR 20D / PXR 25 - t² long delay and flat short delay

Notes:
1. Long delay pickup is 110% of the Ir setting with ±5% tolerance. Ir is set from min to max at steps of 10A.
2. Long delay time settings adjustable from 0.5s to 24s at steps of 0.1s with ±0%/-30% tolerance.
3. If thermal memory is enabled, trip times may be shorter than indicated in this curve.
4. Short delay pickup settings adjustable from 1.5x to 8.0x at steps of 0.1x with ±5% tolerance.
5. Short delay time settings adjustable from 0.050s to 0.500s at steps of 0.010s with tolerances as follows: time delay settings between 0.190s and 0.160s have tolerances of ±10%/-20%, time delay settings between 0.160s and 0.150s have tolerances of ±10%/-30%, and time delay settings between 0.150s and 0.100s have tolerances of ±10%/-40%.
6. If the long delay time is projected to be faster than the short delay time, the long delay trip time will go no faster than the short delay time value.
7. With ZSI enabled and no auxiliary power, tripping times for 3-phase faults will be a maximum of 60ms for 60Hz and 63ms for 50Hz.
Time current curves Power Defense MCCB
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Figure 3. PXR 20 - Iₚt long delay and flat short delay curves

PXR 20 - Iₚt Long Delay and Flat Short Delay Curves

Notes:
1. Long delay pickup is 110% of the Ir setting with ±5% tolerance.
2. Long delay time settings as shown have +0%/-30% tolerance.
3. If thermal memory is enabled, trip times may be shorter than indicated in this curve.
4. Short delay pickup settings as shown have ±5% tolerance.
5. Short delay time settings are shown with tolerances.
6. If the long delay time is projected to be faster than the short delay time, the long delay trip time will go no faster than the short delay time value.
7. With ZSI enabled and no auxiliary power, tripping times for 3-phase faults will be a maximum of 60ms for 60Hz and 63ms for 50Hz.

Time in Seconds

Current in Multiples of Long Delay Setting (Iᵣ)
Time current curves Power Defense MCCB
Frame 4 thermal-magnetic and PXR electronic trip units
Standards: UL, CSA, IEC, CCC

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**Notes:**
1. Long delay pickup is 110% of the Ir setting with ±5% tolerance. Ir is set from min to max at steps of 10 A.
2. Long delay time settings adjustable from 0.5s - 24s at steps of 0.1s with +0%/-30% tolerance.
3. If thermal memory is enabled, trip times may be shorter than indicated in this curve.
4. Short delay pickup settings adjustable from 1.5x - 8.0x at steps of 0.1x with ±5% tolerance.
5. Short Delay Pt slope time settings adjustable from 0.067s - 0.300s at steps of 0.010s with tolerances as follows: Pt slope time delay settings between 0.300s to 0.200s have tolerances of +0/-30%, time delay settings between 0.190s to 0.160s have tolerances of +0/-30%, and time delay settings between 0.150s to 0.100s have tolerances of +0/-40% and time delay settings between 0.090s to 0.067s have tolerances of +0/-50%. After approximately 8x the Pt slope will go flat and those times have tolerances as follows: time delay settings 0.300s to 0.200s have tolerances of +0/-20%, time delay settings between 0.190s to 0.160s have tolerances of +0/-30%, and time delay settings between 0.150s to 0.100s have tolerances of +0/-40% and time delay settings between 0.090s to 0.050s have tolerances of +0/-50%.
6. If the long delay time is projected to be faster than the short delay time, the long delay trip time will go no faster than the short delay trip time value.
7. With ZSI enabled and no auxiliary power, tripping times for 3-phase faults will be a maximum of 66ms for 60Hz and 63ms for 50Hz.

**Current in Multiples of Long Delay Setting (Ir)**

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**Figure 4. PXR 20D / PXR 25 - Pt long delay and Pt short delay**

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**Time current curves Power Defense MCCB**

**Frame 4 thermal-magnetic and PXR electronic trip units**

**Standards:** UL, CSA, IEC, CCC

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**Figure 5. PXR 20 \(i^2t\) long delay and \(i^2t\) short delay Curves**

**Notes:**

1. Long delay pickup is 110% of the \(I_r\) setting with ±5% tolerance.
2. Long delay time settings as shown have ±0%/-30% tolerance.
3. If thermal memory is enabled, trip times may be shorter than indicated in this curve.
4. Short delay pickup settings as shown have ±5% tolerance.
5. Short delay time settings are shown with tolerances.
6. If the long delay time is projected to be faster than the short delay time, the long delay trip time will go no faster than the short delay time value.
7. With ZSI enabled and no auxiliary power, tripping times for 3-phase faults will be a maximum of 60ms for 60Hz and 63ms for 50Hz.

---

**Table:**

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<th>PDF 600 A</th>
<th>PDC 600 A</th>
<th>PDC 1000 A</th>
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Frame 4 thermal-magnetic and PXR electronic trip units
Standards: UL, CSA, IEC, CCC

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Technical Data: PXR 20D / PXR 25 - I't Long Delay and Flat Short Delay Curves

Requirements:
- Style: Frame 4
- Configuration: 3 and 4-poles
- Trip unit type: Power Xpert Release - PXR 20D / PXR 25

Trip characteristics:
- Long delay pickup is 110% of the Ir setting with ±5% tolerance. Ir is set from min to max at steps of 10 A.
- Long delay time settings adjustable from 0.5s - 7s at steps of 0.1s with ±0%/-30% tolerance.
- If thermal memory is enabled, trip times may be shorter than indicated in this curve.
- Short delay pickup settings adjustable from 1.5x - 8.0x at steps of 0.1x with ±5% tolerance.
- Short delay time settings adjustable from 0.050s - 0.500s at steps of 0.010s with tolerances as follows: time delay settings 0.500s to 0.200s have tolerances of +0/-20%, time delay settings between 0.190s to 0.160s have tolerances of +0/-30%, and time delay settings between 0.150s to 0.100s have tolerances of +0/-40% and time delay settings between 0.090s to 0.050s have tolerances of +0/-50%.
- If the long delay time is projected to be faster than the short delay time, the long delay trip time will go no faster than the short delay time value.
- With ZSI enabled and no auxiliary power, tripping times for 3-phase faults will be a maximum of 60ms for 60Hz and 63ms for 50Hz.

Notes:
- Table 1. PXR 20D / PXR 25 - I't Long Delay and Flat Short Delay Curves

<table>
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<th>Ir setting</th>
<th>PDG PDF 800 A</th>
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<th>PDC PDF 1000 A</th>
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<td>Min.</td>
<td>320 A</td>
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<td>Max.</td>
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</table>

Figure 6. PXR 20D / PXR 25 - I't long delay and flat short delay

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Time current curves Power Defense MCCB
Frame 4 thermal-magnetic and PXR electronic trip units
Standards: UL, CSA, IEC, CCC

Notes:
1. Ground pickup settings adjustable from 0.2x - 1.0x at steps of 0.010x for residual sensing with a tolerance of ±10%.
2. Ground time delay settings adjustable from 0.100s – 1.000s at steps of 0.010s with tolerances as follows: time delay settings between 0.190s and 0.160s have tolerances of ±0/-30%, time delay settings between 0.150s and 0.100s have tolerances of ±0/-40%, and time delay settings between 0.010s and 0.200s have tolerances of ±0/+20%.
3. If thermal memory is enabled, trip times may be shorter than indicated in this curve.
4. With ZSI enabled and no auxiliary power, tripping times for 3-phase faults will be a maximum of 60ms for 60Hz and 63ms for 50Hz.
**Technical Data**

**TD012066EN**

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**Time current curves** Power Defense circuit breakers

- **Style:** Frame 4
- **Configuration:** 3 and 4-poles
- **Trip unit type:** Power Xpert Release-PXR 20D / PXR 25

**Notes:**
1. Ground pickup settings adjustable from 0.2x - 1.0x at steps of 0.010x for residual sensing with a tolerance of ±10%.
2. Ground I²t slope time settings are adjustable from 0.067s – 0.300s at steps of 0.010s with tolerances as follows: I²t slope time delay settings 0.300s to 0.200s have tolerances of +0/-30%, time delay settings between 0.190s to 0.160s have tolerances of +0/-30%, and time delay settings between 0.150s to 0.100s have tolerances of +0/-40% and time delay settings between 0.090s to 0.067s have tolerances of +20%/-50%. After approximately 1x the I²t slope will go flat and those times have tolerances as follows: Time delay settings 0.300s to 0.200s have tolerances of +0/-20%, time delay settings between 0.190s to 0.160s have tolerances of +0/-30%, and time delay settings between 0.150s to 0.100s have tolerances of +0/-40% and time delay settings between 0.090s to 0.067s have tolerances of +20%/-50%.
3. Ground pickup settings adjustable from 0.2x - 1.0x at steps of 0.010x for residual sensing with a tolerance of ±10%.
4. Ground I²t slope time settings are adjustable from 0.067s – 0.300s at steps of 0.010s with tolerances as follows: I²t slope time delay settings 0.300s to 0.200s have tolerances of +0/-30%, time delay settings between 0.190s to 0.160s have tolerances of +0/-30%, and time delay settings between 0.150s to 0.100s have tolerances of +0/-40% and time delay settings between 0.090s to 0.067s have tolerances of +20%/-50%.
5. If thermal memory is enabled, trip times may be shorter than indicated in this curve.
6. With ZSI enabled and no auxiliary power, tripping times for 3-phase faults will be a maximum of 60ms for 60Hz and 63ms for 50Hz.

**Figure 8. PXR 20D / PXR 25 - ground (earth) I²t delay curve**
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Frame 4 thermal-magnetic and PXR electronic trip units
Standards: UL, CSA, IEC, CCC

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Figure 9. PXR 20 - ground (earth) flat delay

Notes:
1. Ground pickup settings as shown are for residual sensing with a tolerance of ±10%.
2. Ground slope flat time setting are shown with tolerances.
3. If thermal memory is enabled, trip times may be shorter than indicated in this curve.
4. With ZSI enabled and no auxiliary power, tripping times for 3-phase faults will be a maximum of 60ms for 60Hz and 63ms for 50Hz.
Time current curves
Power Defense circuit breakers
Style: Frame 4
Configuration: 3 and 4-poles
Trip unit type: Power Xpert Release-PXR 20

Notes:
1. Ground pickup settings as shown are for residual sensing with a tolerance of ±10%.
2. Ground I^2t flat time setting are shown with tolerances.
3. If thermal memory is enabled, trip times may be shorter than indicated in this curve.
4. With ZSI enabled and no auxiliary power, tripping times for 3-phase faults will be a maximum of 60ms for 60Hz and 63ms for 50Hz.

Figure 10. PXR 20 - ground (earth) I^t delay

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Frame 4 thermal-magnetic and PXR electronic trip units
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Figure 11. PXR 20D / PXR 25 - instantaneous and override for 800A frame

Notes:
1. The instantaneous pickup settings adjustable from 2x – 8.5x(max) at steps of 0.10x with ±10% tolerance.
2. For high fault current levels a fixed instantaneous override is provided at 8600 A and has a ±15% tolerance.

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Figure 12. PXR 20D / PXR 25 - instantaneous (1000A)

**Notes:**
1. The instantaneous pickup settings adjustable from 2x – 8x(max) at steps of 0.10x with ±10% tolerance.
2. For high fault current levels a fixed instantaneous override is provided at 8000 A and has ±15% tolerance.
Time current curves Power Defense circuit breakers

Style: Frame 4
Configuration: 3 and 4-poles
Trip unit type: Power Xpert Release-PXR 20 / PXR 10

Notes:
1. The instantaneous pickup settings as shown with a ±10% tolerance.
2. For high fault current levels a fixed instantaneous override is provided at 8000 A and has a ±15% tolerance.
Figure 14. PXR 20 / PXR 10 - instantaneous and override 1000A frame
**PXR 20 / PXR 20D / PXR 25 - Maintenance Mode Curves**

**Notes:**
1. Maintenance mode pickup settings have a ±20% tolerance.

---

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Time current curves
Power Defense circuit breakers
Style: Frame 4
Configuration: 3 and 4-poles
Trip unit type: Power Xpert Release-PXR 20 / PXR 20D / PXR 25

---

**Figure 15. PXR 20 / PXR 20D / PXR 25 - maintenance mode**

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**Time current curves Power Defense circuit breakers**
Style: Frame 4
Configuration: 3 and 4-poles
Trip unit type: Power Xpert Release -PXR 10
Trip unit style: LI

- **Ir setting**
- **PDG PDF 800 A**
- **PDC 800 A**

<table>
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<tr>
<td>10</td>
<td>800 A</td>
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</tr>
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</table>

**Notes:**
1. Long delay pickup is 110% of the Ir setting with ±5% tolerance.
2. Long delay time settings have ±0%/-30% tolerance.
3. Instantaneous pickup settings have ±10% tolerance.
4. For high fault current levels a fixed instantaneous override is provided at 6800 A and has ±15% tolerance.
5. If thermal memory is enabled, trip times may be shorter than indicated in this curve.
Time current curves Power Defense circuit breakers
Style: Frame 4
Configuration: 3 and 4-poles
Trip unit type: Power Xpert Release -PXR 10
Trip unit style: LI

Ir setting  PDC 1000 A
1  400 A
2  550 A
3  630 A
4  700 A
5  750 A
6  800 A
7  850 A
8  900 A
9  950 A
10 1000 A

Notes:
1. Long delay pickup is 110% of the Ir setting with ±5% tolerance.
2. Long delay time settings has ±0%/-30% tolerance.
3. Instantaneous pickup settings have ±10% tolerance.
4. For high fault current levels a fixed instantaneous override is provided at 8000 A and has a ±15% tolerance.
5. If thermal memory is enabled, trip times may be shorter than indicated in this curve.

Figure 17. PXR 10 LI 1000A frame
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Figure 18. PXR 10 LSI profile for short flat curves
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Figure 19. PXR 10 LSI profile for I^2t short curves

Notes:
1. Long delay pickup is 110% of the Ir setting with ±5% tolerance.
2. Long delay time setting has +0%/-30% tolerance.
3. Instantaneous pickup settings have ±10% tolerance.
4. Short delay pickup settings as shown have ±5% tolerance.
5. If thermal memory is enabled, trip times may be shorter than indicated in this curve.
6. Profile J is set at a default value of 8x with 300ms time delay but is programmable with Isd 2.0x to 8.0x in steps of 0.5x and tsd 50ms to 300ms in steps of 50ms and I^2t slope as an option.
7. When profile K is selected, PXR10 LSI style curve should be used.
8. Setting J in the table is the default value but can be programmed from a minimum of 2x to a maximum of 8x in steps of 0.5x and a time delay of 50ms to 300ms in steps of 50ms using the Power Xpert Protection Manager software (PXPM).
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Figure 20. Fixed thermal adjustable magnetic 300A-600A

Notes:
1. Utilization category A
   \( U_{IM} = 8kV \)
2. DC instantaneous trip values are approximately 40% higher.
3. Magnetic settings are a multiple of In rating.
4. Thermal setting is a function of Ir setting or rating.
Figure 21. Fixed thermal adjustable magnetic 700A-800A
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Figure 22. Adjustable thermal adjustable magnetic 630A-1000A

Notes:
1. Utilization category A
   \[ U_{\text{imp}} = 8kV \]
2. DC instantaneous trip values are approximately 40% higher.
3. Magnetic settings are a multiple of In rating.
4. Thermal setting is a function of Ir setting or rating.
5. The Ir adjustment range is 100% to 80% of In.
Figure 23. 240V let through current

PD4 800A 240V
Peak Let Through Current

Available Short Circuit Current, kA_{rms}
Figure 24. 240V peak let through energy
Figure 25. 415V-480V let through current

PD4 800A 415V-480V
Peak Let Through Current

Available Short Circuit Current, kA\textsubscript{rms}
Time current curves Power Defense MCCB
Frame 4 thermal-magnetic and PXR electronic trip units
Standards: UL, CSA, IEC, CCC

Figure 26. 415V-480V let through energy

PD4 800A 415V - 480V
Peak Let Through Energy

Available Short Circuit Current, kA rms

Peak Let Through Energy $I^2t$, A$^2$ sec

415V - 480V

Figure 26. 415V-480V let through energy

November 2019
Figure 27. 600V let through current
Time current curves Power Defense MCCB
Frame 4 thermal-magnetic and PXR electronic trip units
Standards: UL, CSA, IEC, CCC

Figure 28. 600V let through energy

Peak Let Through Energy

Available Short Circuit Current, kA rms

Eaton Corporation
September 2017  Rev. 1

Figure 28. 600V let through energy

November 2019
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Time current curves Power Defense MCCB
Frame 4 thermal-magnetic and PXR electronic trip units
Standards: UL, CSA, IEC, CCC