Technical Data **TD012065EN**

Effective January 2025
Supersedes November 2019

Time current curves Power Defense MCCB Frame 3 thermal-magnetic and PXR electronic trip units Standards: UL, CSA, IEC, CCC

Contents

Powering Business Worldwide

Thermal magnetic trip unit curves

Peak let through curves

Table 1. Revision notes

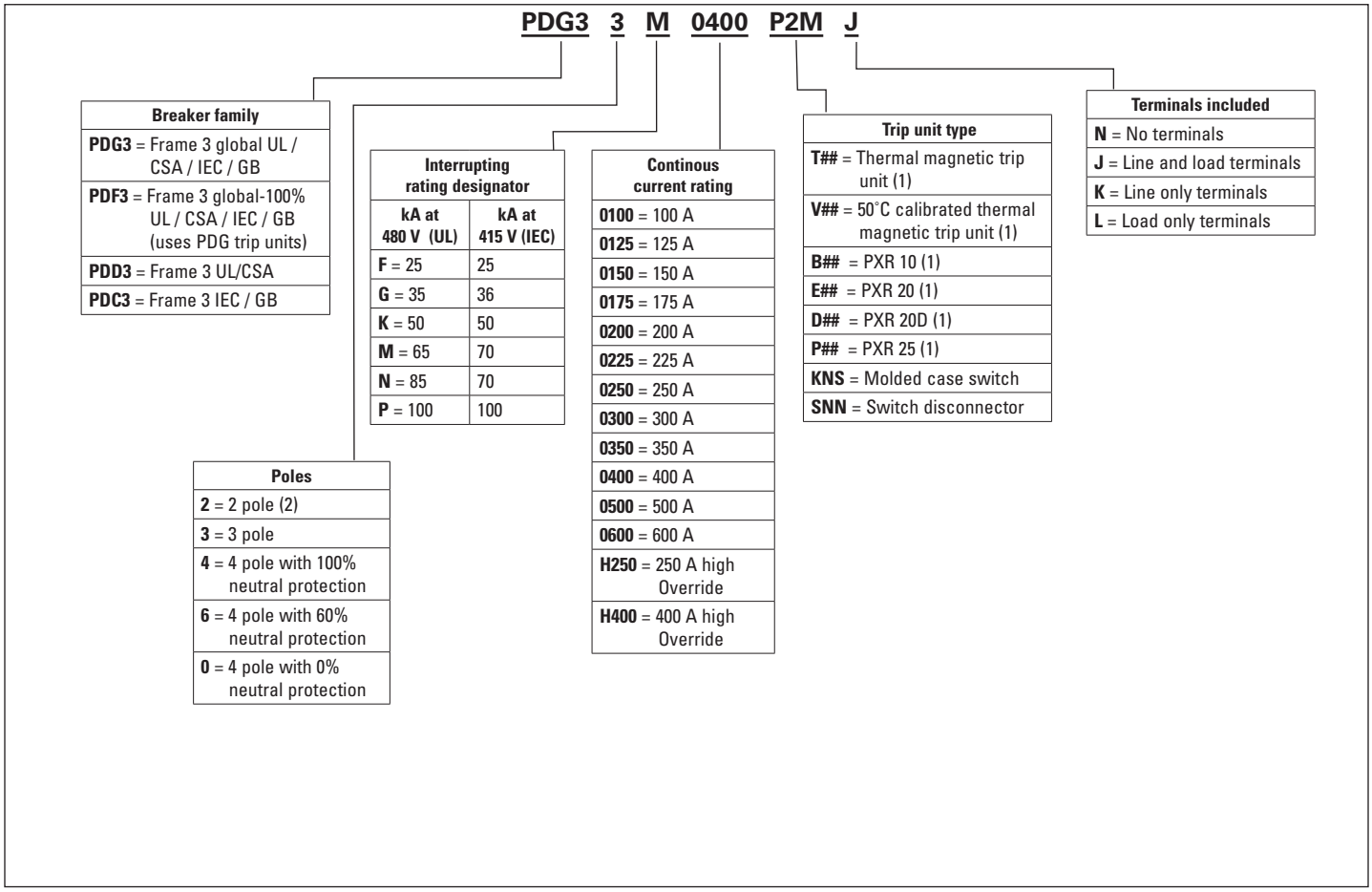
Note: Unless noted below, all curves remain unchanged from their prior revision.

Revision		Curve number	Page	Date
1	Power Defense frame 3 initial release.			02/12/2019
2	Short delay tolerances adjusted for phase and ground on I^2t slopes.			11/2019
3	Update time current curves and corresponding table for PXR 10 in a PD3.	Figure 33.	39	01/27/2025

This information is provided only as an aid to understand the catalog numbers.

It is not to be used to build catalog numbers for circuit breakers or trip units as all combinations may not be available.

Table 2. Circuit breaker catalog number convention

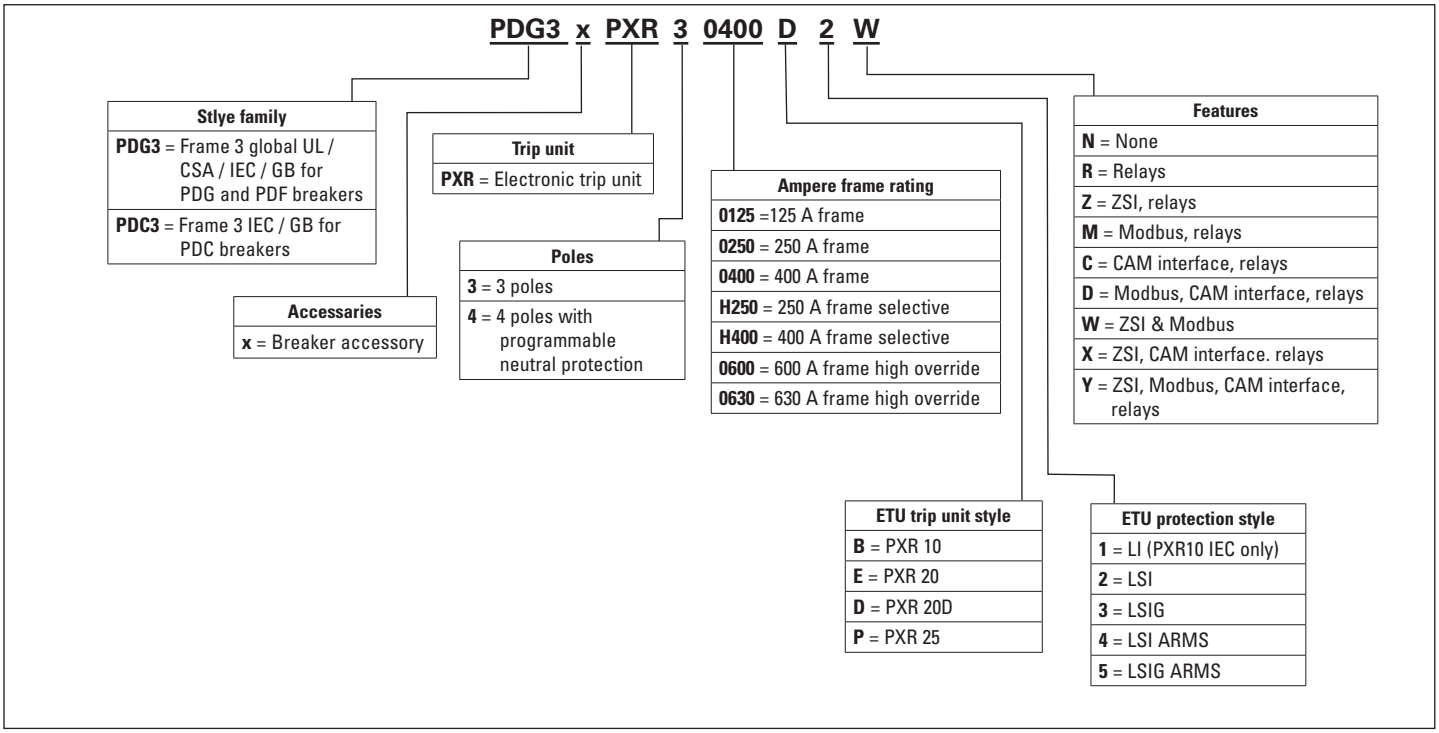


Note: 1 See catalog for ## (protection type and available configured options)

Note: 2 All PD-3 2-pole breakers are physically the same size as a 3-pole frame with the outer poles used for electrical connections.

Note: 3 IEC standard breakers include the CE mark; GB standard breakers include the CCC mark.

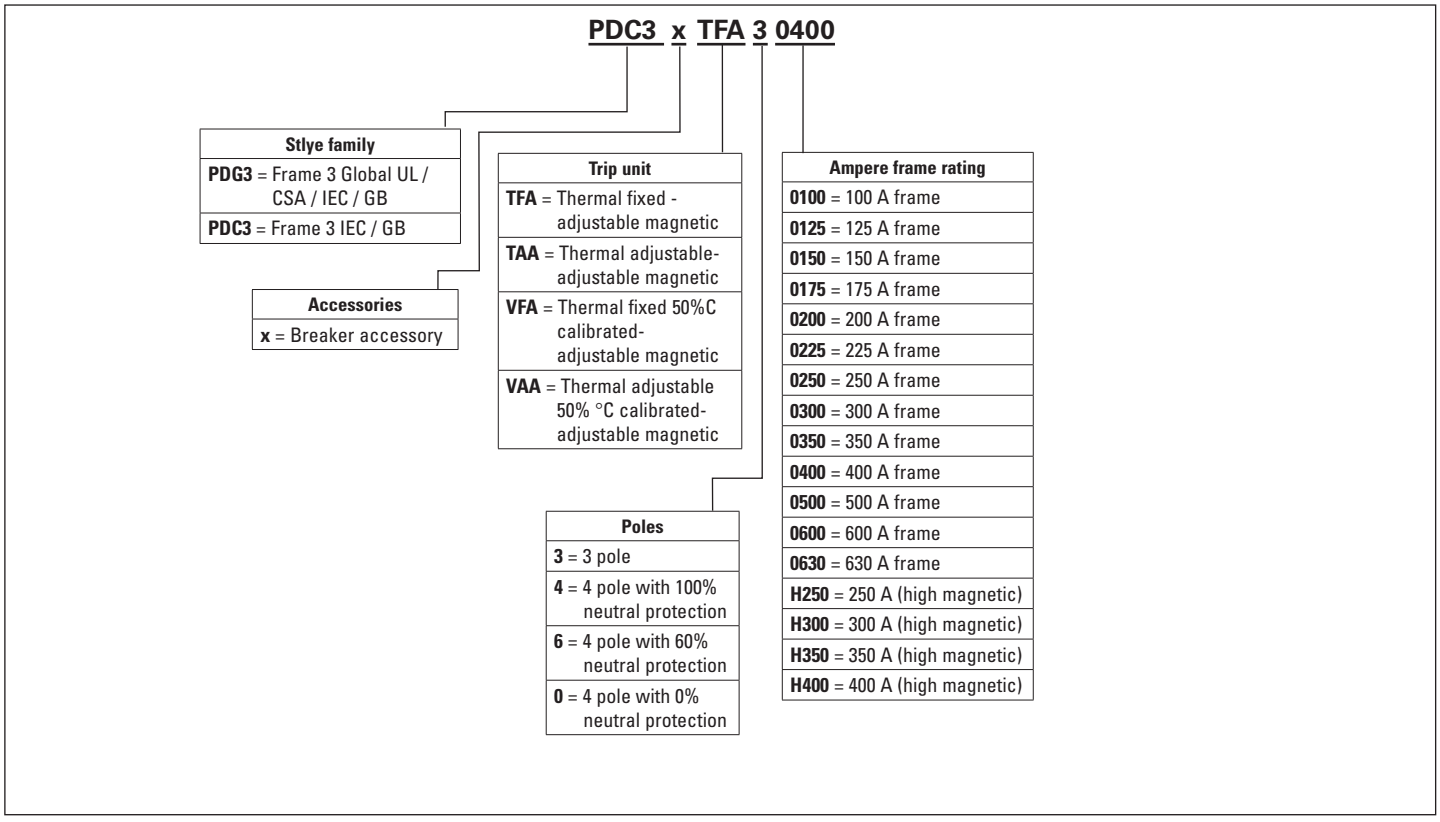
Table 3. Electronic trip unit catalog number convention



Note: IEC standard breakers include the CE mark; GB standard breakers include the CCC mark.

Note: The Selective frame styles have a higher override value for higher selective coordination capability.

Table 4. Thermal magnetic trip unit catalog number convention



Note: IEC standard breakers include the CE mark; GB standard breakers include the CCC mark.

Table 5. Symmetrical RMS interruption ratings I_{cu} (kA) for each breaker frame

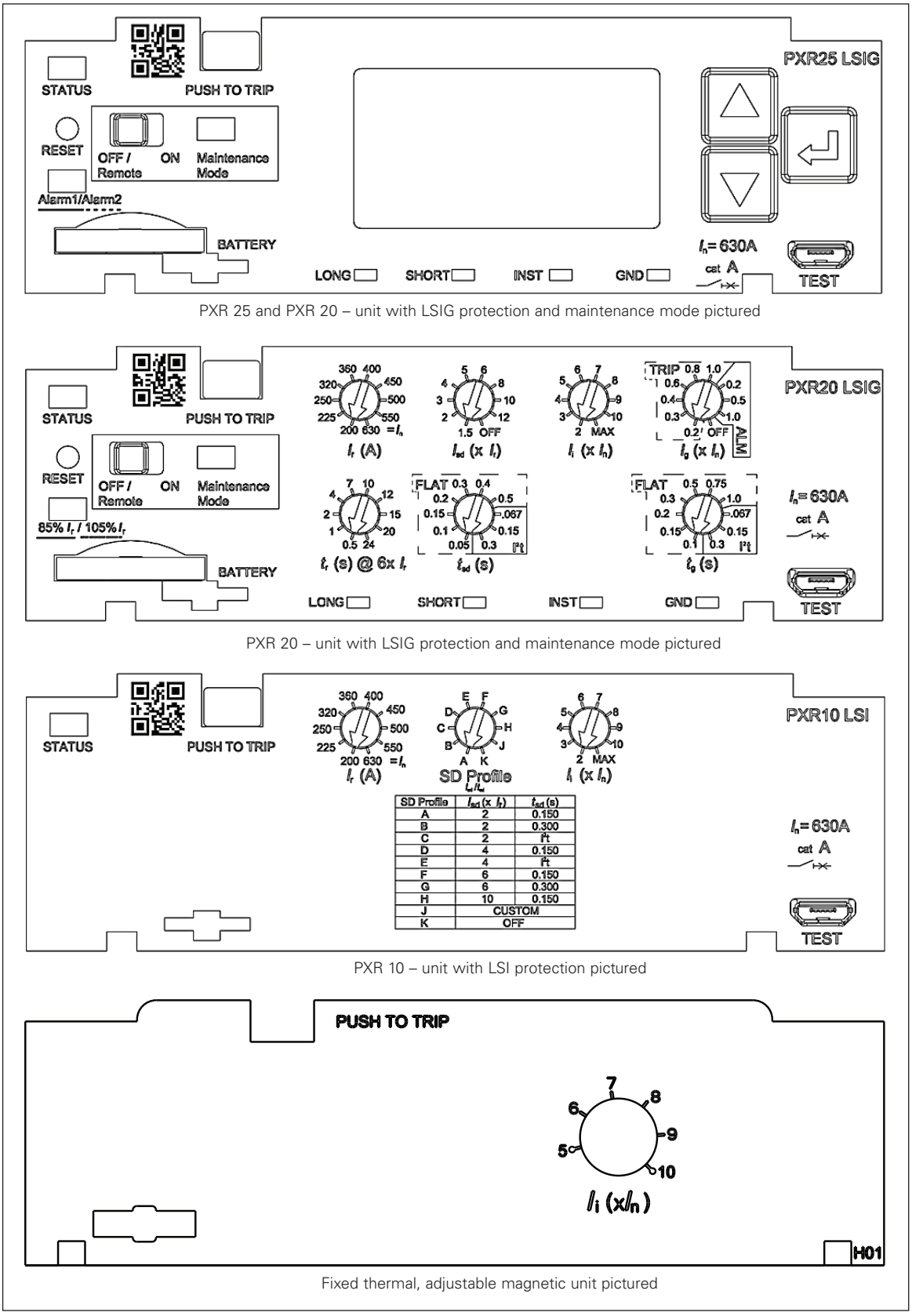
		UL / CSA			IEC / CCC							
	Voltage / Frame	240V	480V	600V	240V	415V	440V	480V	525V	690V	250 Vdc* 400A frame	250 Vdc* 600A/630A frame
Globally rated	PDG3xF	35	25	14	35	25	25	20	18	-	10	22
	PDG3xG	65	35	18	55	36	30	25	20	8	10	22
	PDG3xK	85	50	25	85	50	35	35	25	10	10	22
	PDG3xM	100	65	35	100	70	50	50	30	15	22	42
	PDG3xN	150	85	50	150	70	70	65	35	20	22	42
	PDG3xP	200	100	65	200	100	100	85	40	20	22	42
Globally rated (UL 100%)	PDF4xF	35	25	14	35	25	25	20	18	-	10	22
	PDF4xG	65	35	18	55	36	30	25	20	8	10	22
	PDF4xK	85	50	25	85	50	35	35	25	10	10	22
	PDF4xM	100	65	35	100	70	50	50	30	15	22	42
IEC / GB only	PDC3xF	-	-	-	35	25	25	20	18	-	10	22
	PDC3xG	-	-	-	55	36	30	25	20	8	10	22
	PDC3xK	-	-	-	85	50	35	35	25	10	10	22
	PDC3xM	-	-	-	100	70	50	50	30	15	22	42
	PDC3xN	-	-	-	150	70	70	65	35	20	22	42
UL/CSA Up to 240V	PDD3xF	35	-	-	-	-	-	-	-	-	10	22
	PDD3xG	65	-	-	-	-	-	-	-	-	10	22
	PDD3xK	85	-	-	-	-	-	-	-	-	10	22
	PDD3xM	100	-	-	-	-	-	-	-	-	22	42
	PDD3xN	150	-	-	-	-	-	-	-	-	22	42
	PDD3xP	200	-	-	-	-	-	-	-	-	22	42

* Two poles in series

Table 6. Curve notes

1.	These curves apply for 50Hz and 60Hz applications
2.	The maximum voltage rating for the frame style is stated in Table 5.
3.	These curves are comprehensive for Power Defense style circuit breakers including frame sizes, ratings and constructions stated.
4.	The total clearing times shown include the response time for the trip unit, the breaker opening and the interruption of the current. The bottom of the time band is the minimum commit to trip time.
5.	The end of the curve is determined by the application or the interrupting rating of the circuit breaker.
6.	Thermal Magnetic trip unit calibration based on 40ºC ambient, cold start. Tested with 4 feet of rated wire (75ºC) per terminal. Tested in open air with current in all poles.
7.	Thermal Magnetic trip unit instantaneous calibration based on single pole testing.
8.	All electronic trip units have an over temperature protection feature that will trip the breaker when the internal temperature of the ETU is over 105ºC.
9	All time current data for PXR is based on 3 phase testing.

Labels



SD Profile	I_{sd} (x I_r)	t_{sd} (s)
A	2	0.150
B	2	0.300
C	2	I^2t
D	4	0.150
E	4	I^2t
F	6	0.150
G	6	0.300
H	10	0.150
J	CUSTOM	
K	OFF	

PXR 25 and PXR 20 – unit with LSIG protection and maintenance mode pictured

PXR 20 – unit with LSIG protection and maintenance mode pictured

PXR 10 – unit with LSI protection pictured

Fixed thermal, adjustable magnetic unit pictured

Figure 1. Power Defense frame 3 trip unit front labels.

Note: Trip unit drawings in Figure 1 are representative of the face plates provided. Values on the trip unit dials will change based upon the specific breaker and trip unit. Refer to the time current curve of the breaker or the PXR User Guide for the specific settings.

Curves

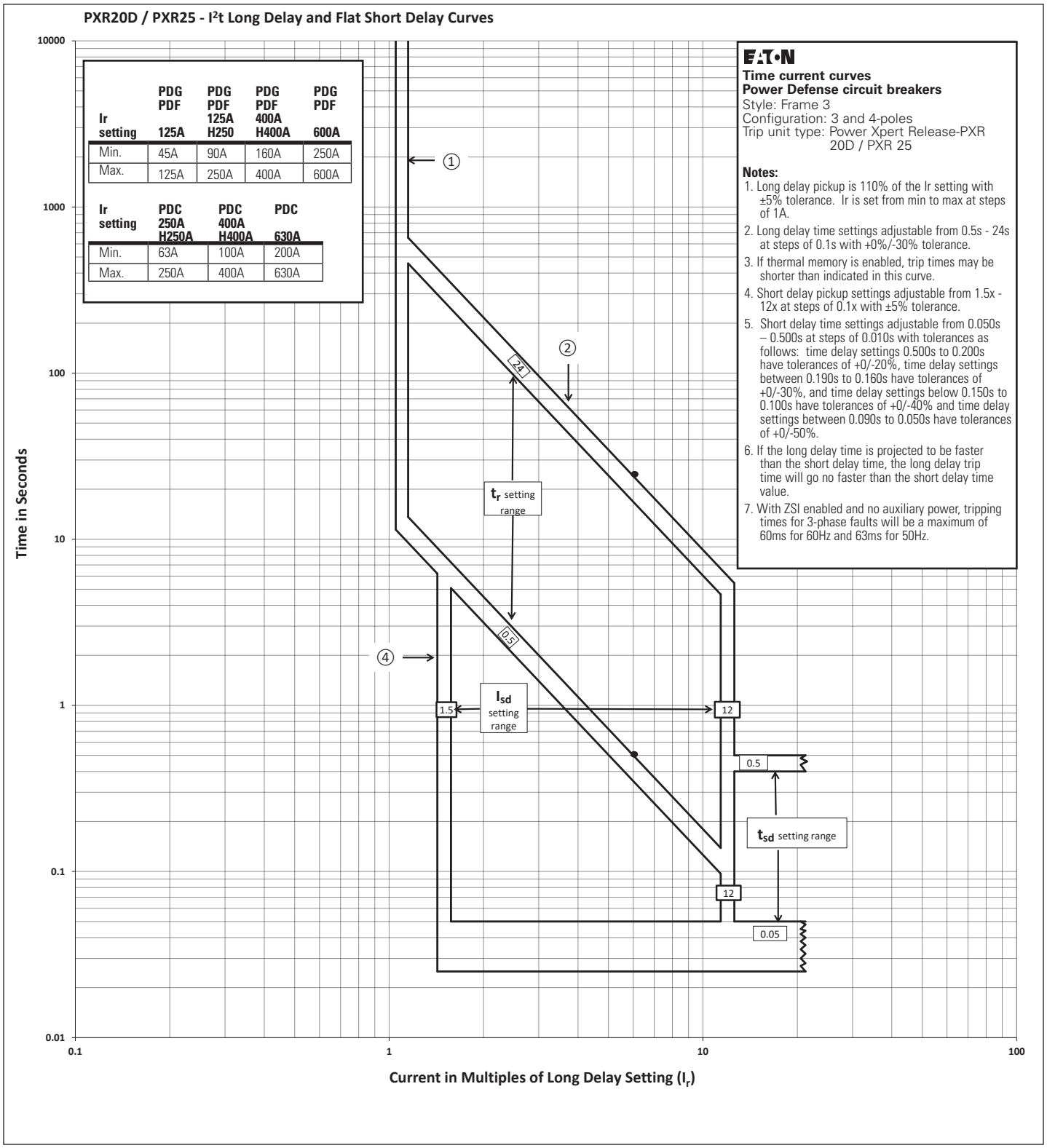
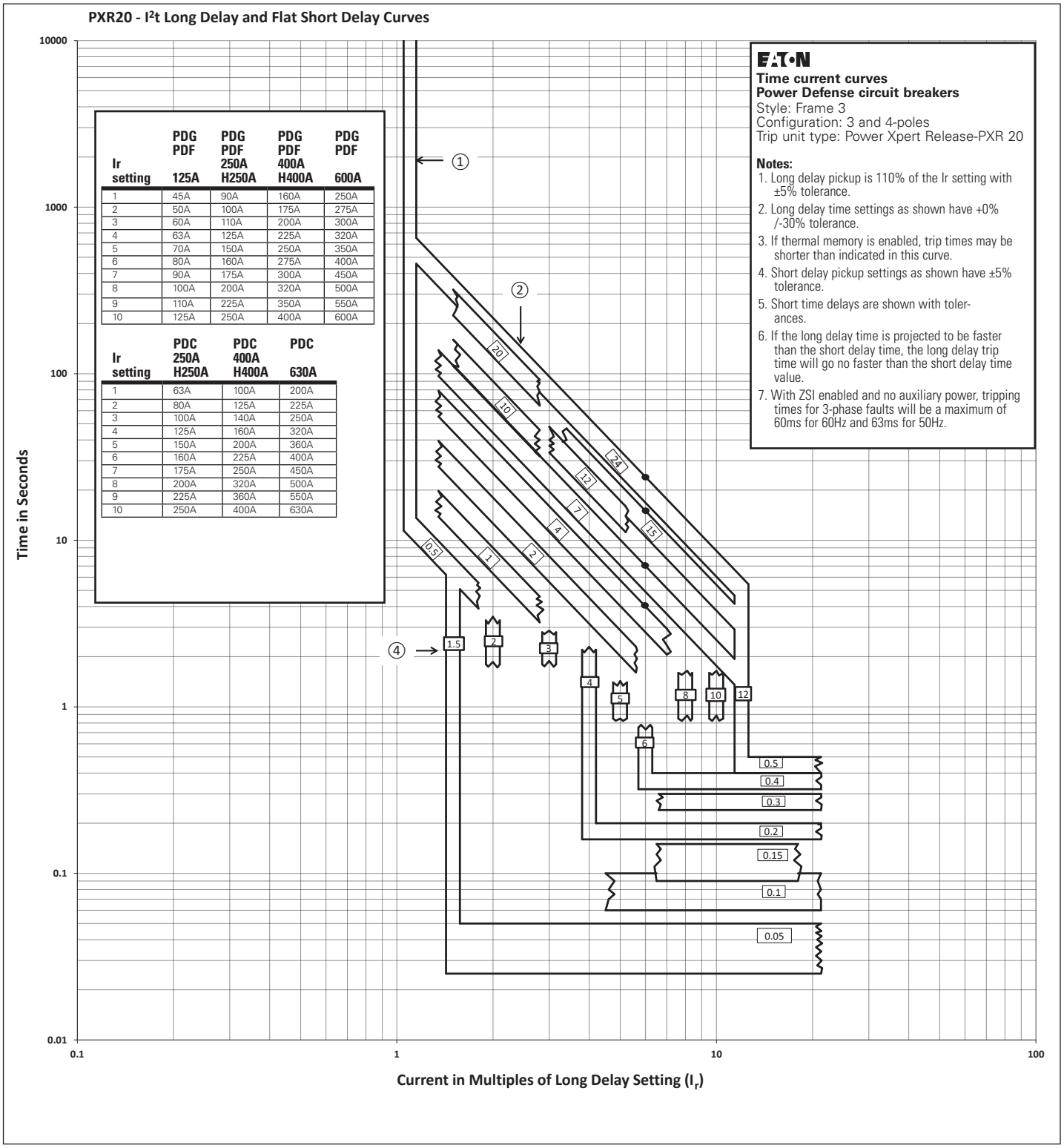


Figure 2. PXR 20D / PXR 25 - I²t long delay and flat short delay. **January 2025**



Ir setting	PDG PDF 125A	PDG PDF 250A H250A	PDG PDF 400A H400A	PDG PDF 600A
1	45A	90A	160A	250A
2	50A	100A	175A	275A
3	60A	110A	200A	300A
4	63A	125A	225A	320A
5	70A	150A	250A	350A
6	80A	160A	275A	400A
7	90A	175A	300A	450A
8	100A	200A	320A	500A
9	110A	225A	350A	550A
10	125A	250A	400A	600A

Ir setting	PDC 250A H250A	PDC 400A H400A	PDC 630A
1	63A	100A	200A
2	80A	125A	225A
3	100A	140A	250A
4	125A	160A	320A
5	150A	200A	360A
6	160A	225A	400A
7	175A	250A	450A
8	200A	320A	500A
9	225A	360A	550A
10	250A	400A	630A

Time current curves
Power Defense circuit breakers
Style: Frame 3
Configuration: 3 and 4-poles
Trip unit type: Power Xpert Release-PXR 20

Notes:
1. Long delay pickup is 110% of the Ir setting with ±5% tolerance.
2. Long delay time settings as shown have +0% /-30% tolerance.
3. If thermal memory is enabled, trip times may be shorter than indicated in this curve.
4. Short delay pickup settings as shown have ±5% tolerance.
5. Short time delays are shown with tolerances.
6. If the long delay time is projected to be faster than the short delay time, the long delay trip time will go no faster than the short delay time value.
7. With ZSI enabled and no auxiliary power, tripping times for 3-phase faults will be a maximum of 60ms for 60Hz and 63ms for 50Hz.

Figure 3. PXR 20 - I²t long delay and flat short delay.

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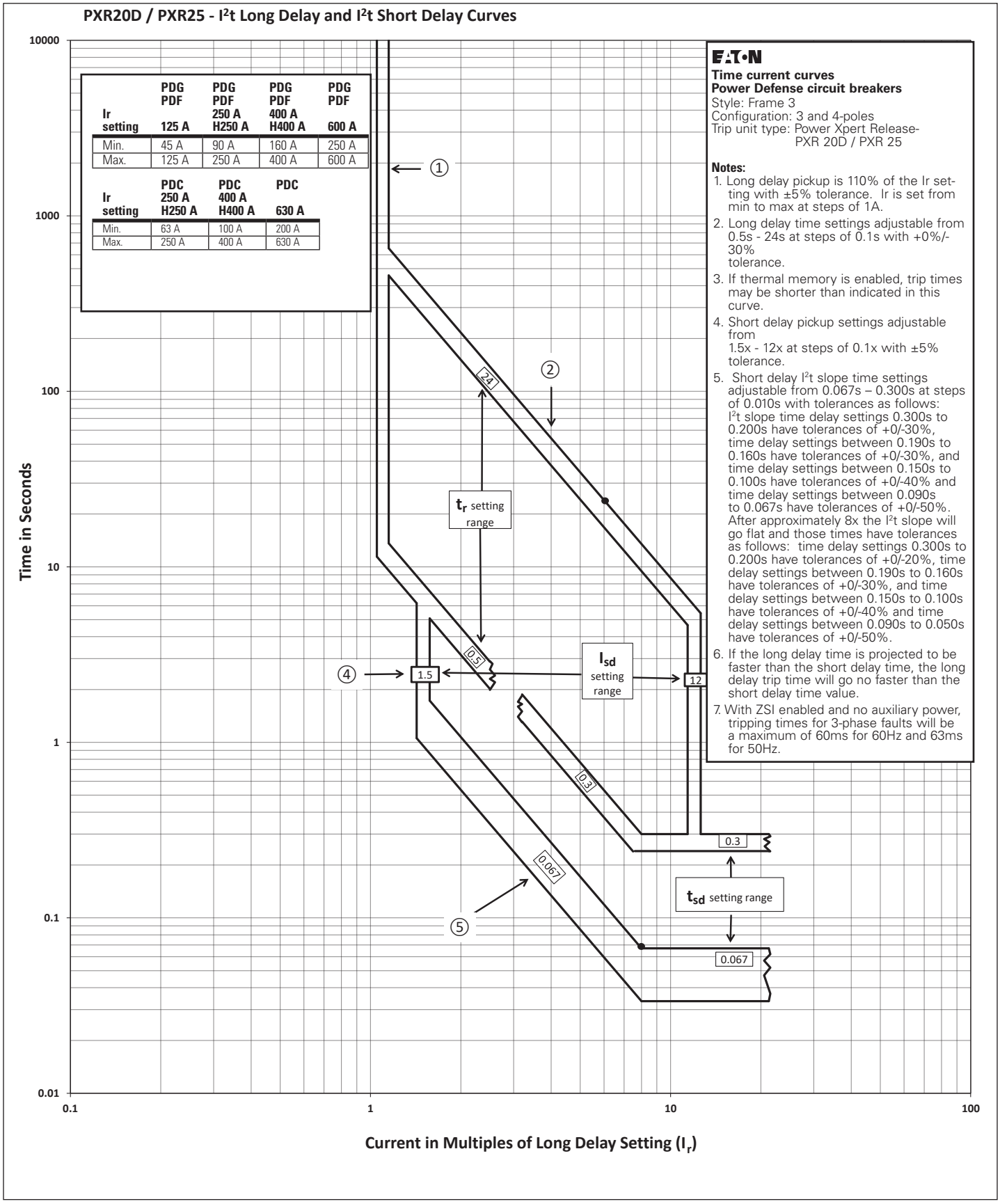

Figure 4. PXR 20D / PXR 25 - I²t long delay and I²t short delay. **January 2025**

PXR20 - I²t Long Delay and I²t Short Delay Curves

Ir setting	PDG PDF 125A	PDG PDF 250A H250A	PDG PDF 400A H400A	PDG PDF 600A
1	45A	90A	160A	250A
2	50A	100A	175A	275A
3	60A	110A	200A	300A
4	63A	125A	225A	320A
5	70A	150A	250A	350A
6	80A	160A	275A	400A
7	90A	175A	300A	450A
8	100A	200A	320A	500A
9	110A	225A	350A	550A
10	125A	250A	400A	600A

Ir setting	PDC 250A H250A	PDC 400A H400A	PDC 630A
1	63A	100A	200A
2	80A	125A	225A
3	100A	140A	250A
4	125A	160A	320A
5	150A	200A	360A
6	160A	225A	400A
7	175A	250A	450A
8	200A	320A	500A
9	225A	360A	550A
10	250A	400A	630A

Time current curves
Power Defense circuit breakers
Style: Frame 3
Configuration: 3 and 4-poles
Trip unit type: Power Xpert Release-PXR 20

Notes:
1. Long delay pickup is 110% of the Ir setting with ±5% tolerance.
2. Long delay time settings as shown have +0% /-30% tolerance.
3. If thermal memory is enabled, trip times may be shorter than indicated in this curve.
4. Short delay pickup settings as shown have ±5% tolerance.
5. Short delay I²t slope time settings are as follows: I²t slope time delay setting 0.300s has a tolerance of +0/-30%, time delay setting 0.150s has a tolerance of +0/-40% and time delay setting 0.067s has a tolerance of +0/-50%. After approximately 8x the I²t slope will go flat and those times have tolerances as follows: time delay setting 0.300s has a tolerance of +0/-20%, time delay setting 0.150s has a tolerance of +0/-40% and time delay setting 0.067s has a tolerance of +0/-50%.
6. If the long delay time is projected to be faster than the short delay time, the long delay trip time will go no faster than the short delay time value.
7. With ZSI enabled and no auxiliary power, tripping times for 3-phase faults will be a maximum of 60ms for 60Hz and 63ms for 50Hz.

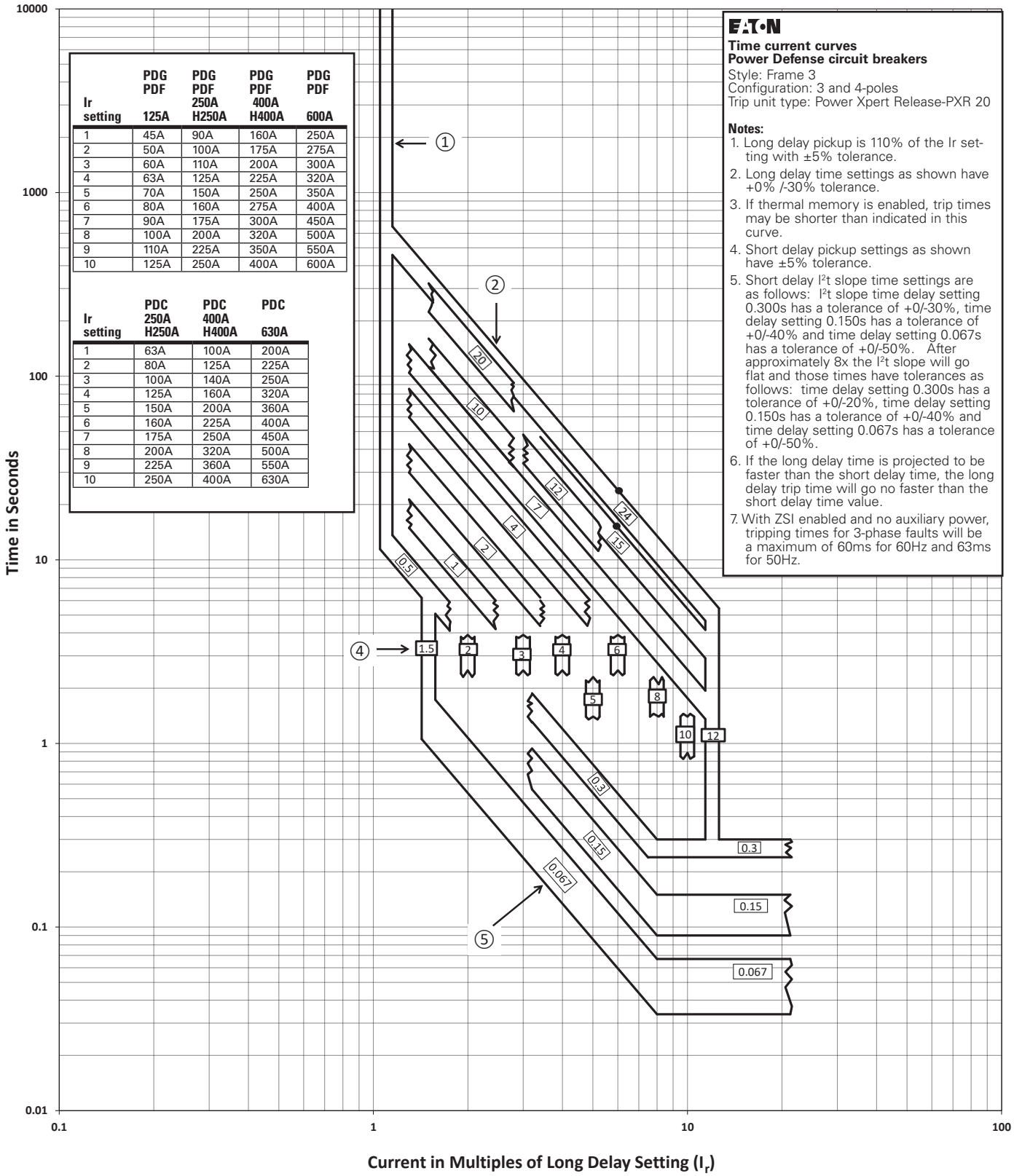

Figure 5. PXR 20 I²t long delay and I²t short delay.

January 2025

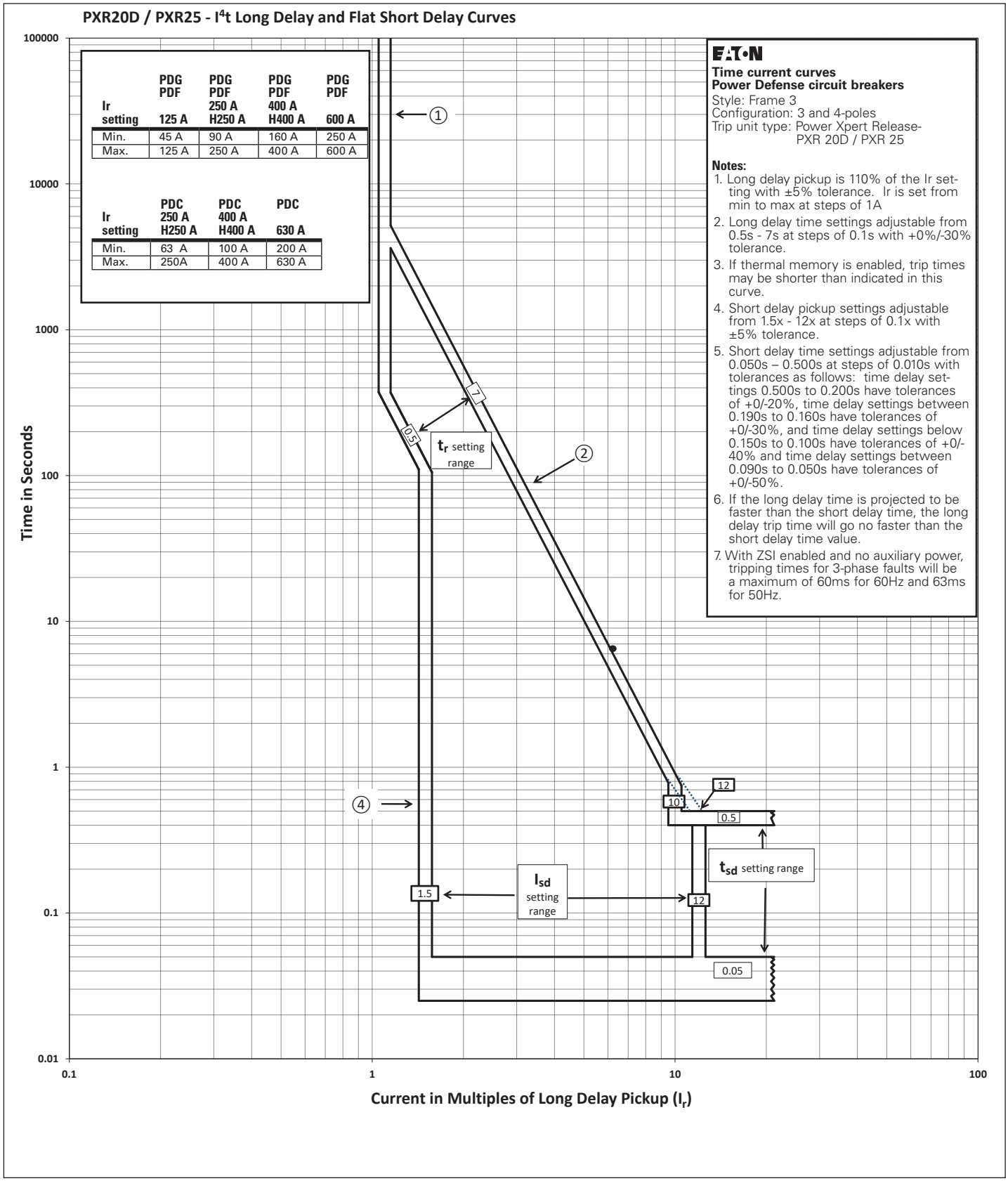

Figure 6. PXR 20D / PXR 25 - I4t long delay and flat short delay.

January 2025

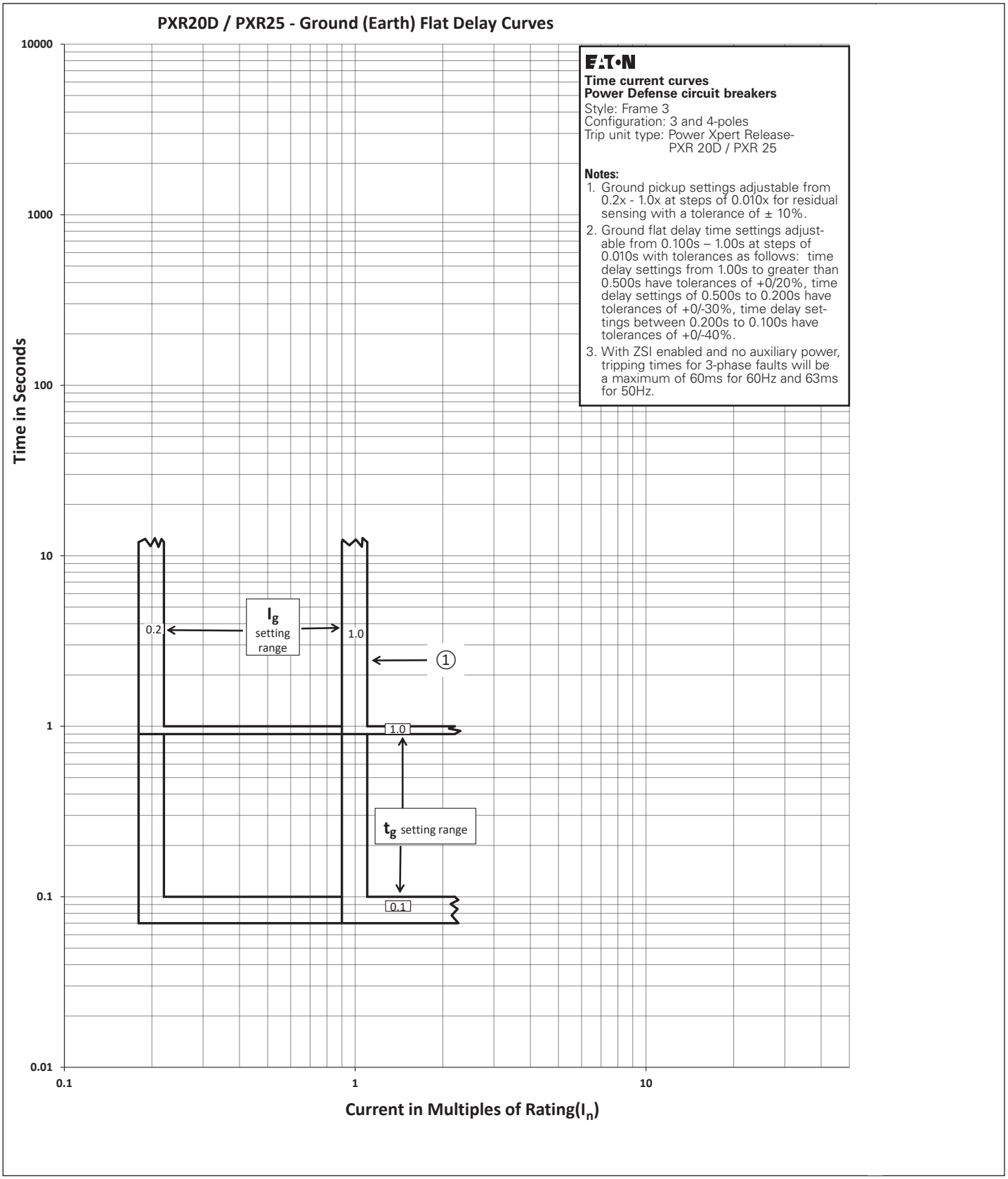

Figure 7. PXR 20D / PXR 25 ground (earth) flat delay.

January 2025

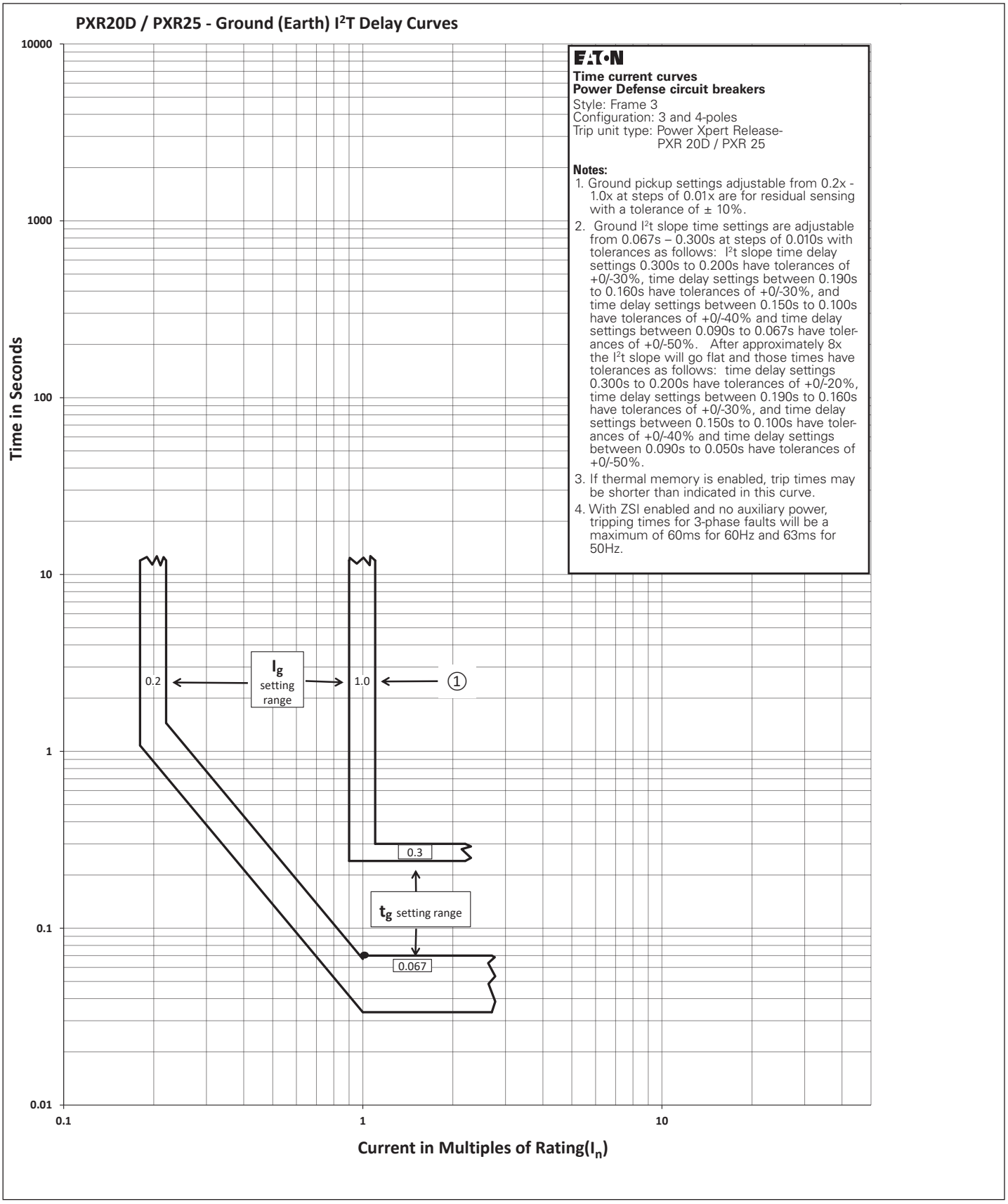

Figure 8. PXR 20D / PXR 25 -ground (earth) I²t delay.

January 2025

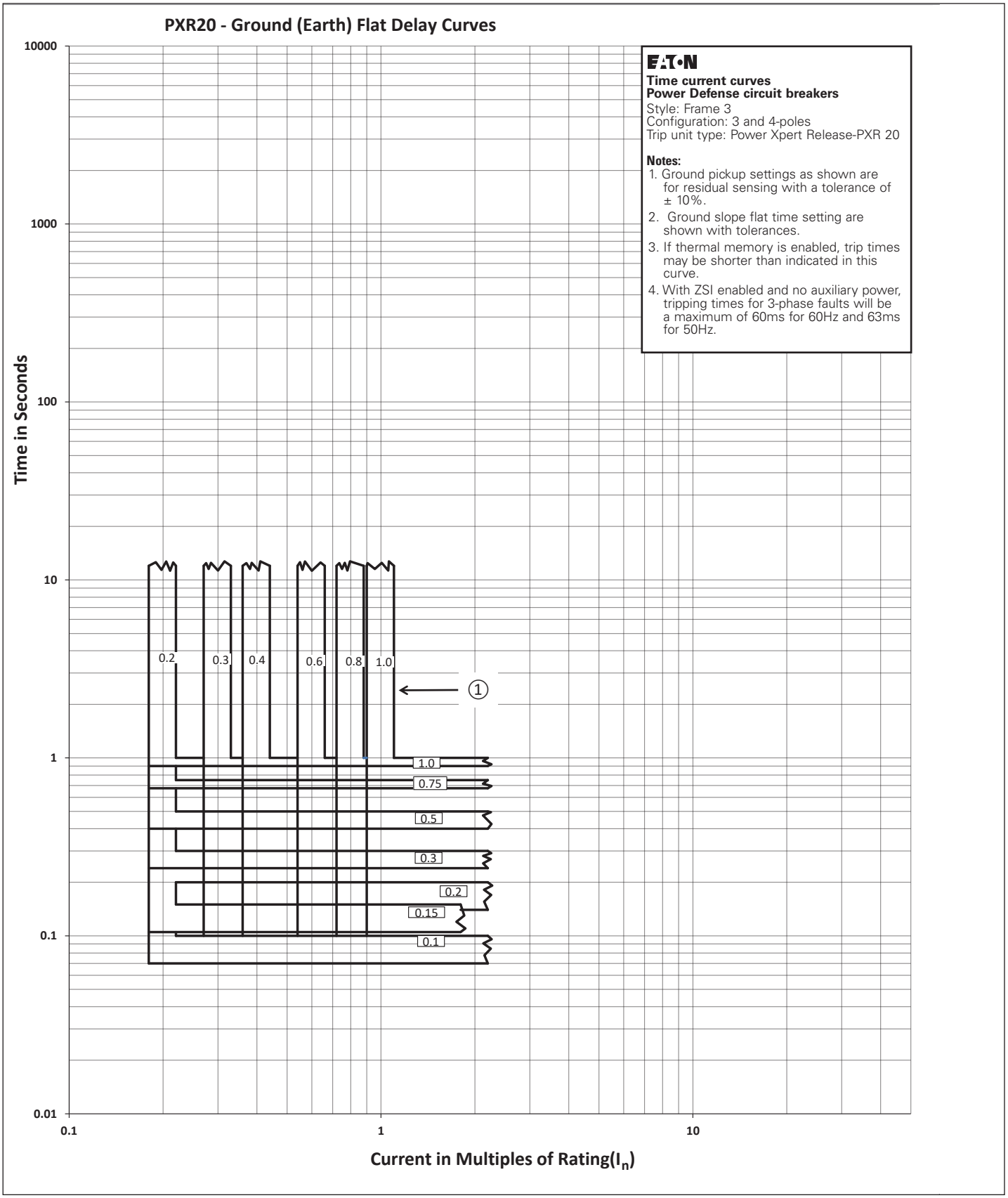

Figure 9. PXR 20 - ground (earth) flat delay.

January 2025

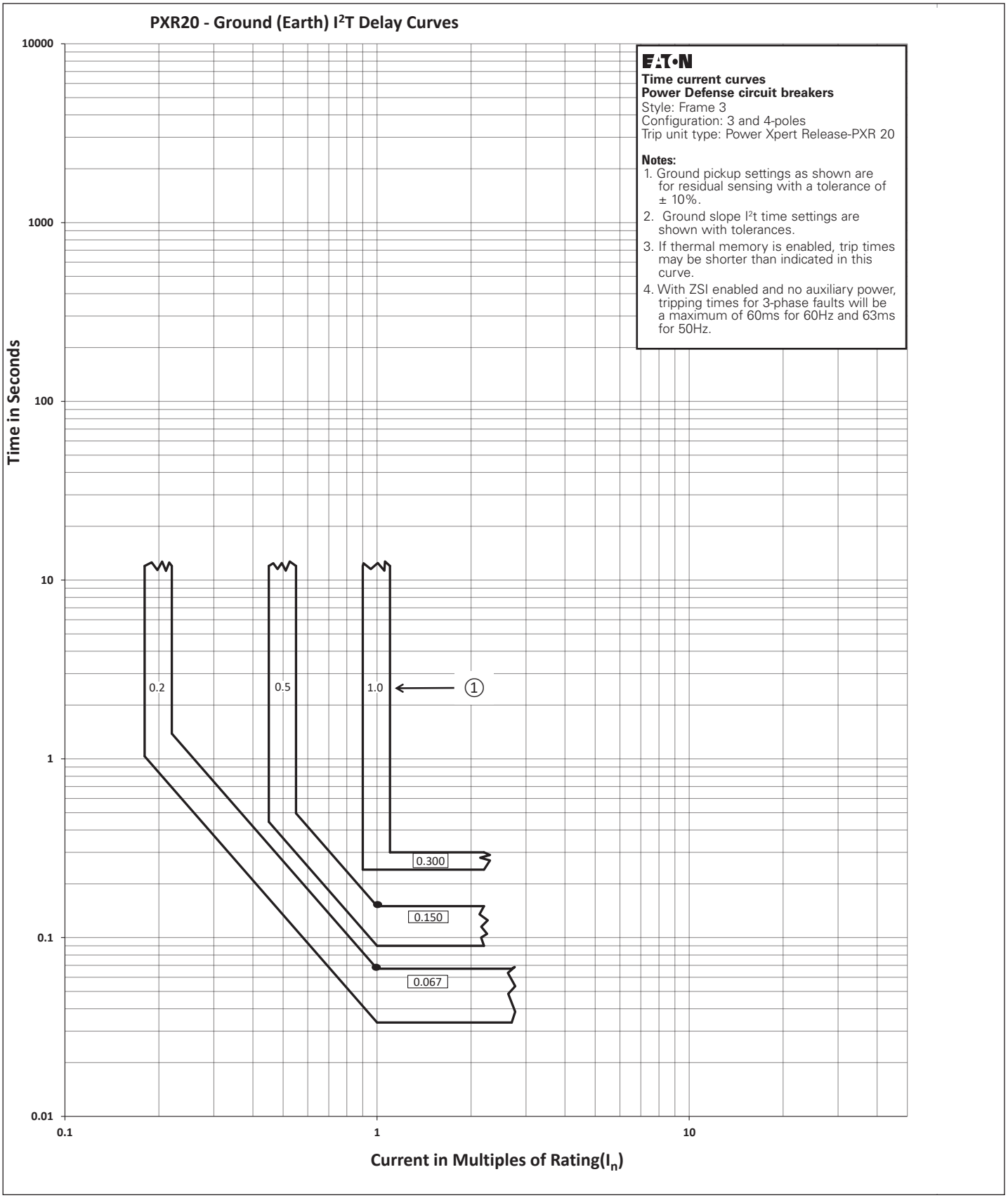

Figure 10. PXR 20 - ground (earth) I²t delay.

January 2025

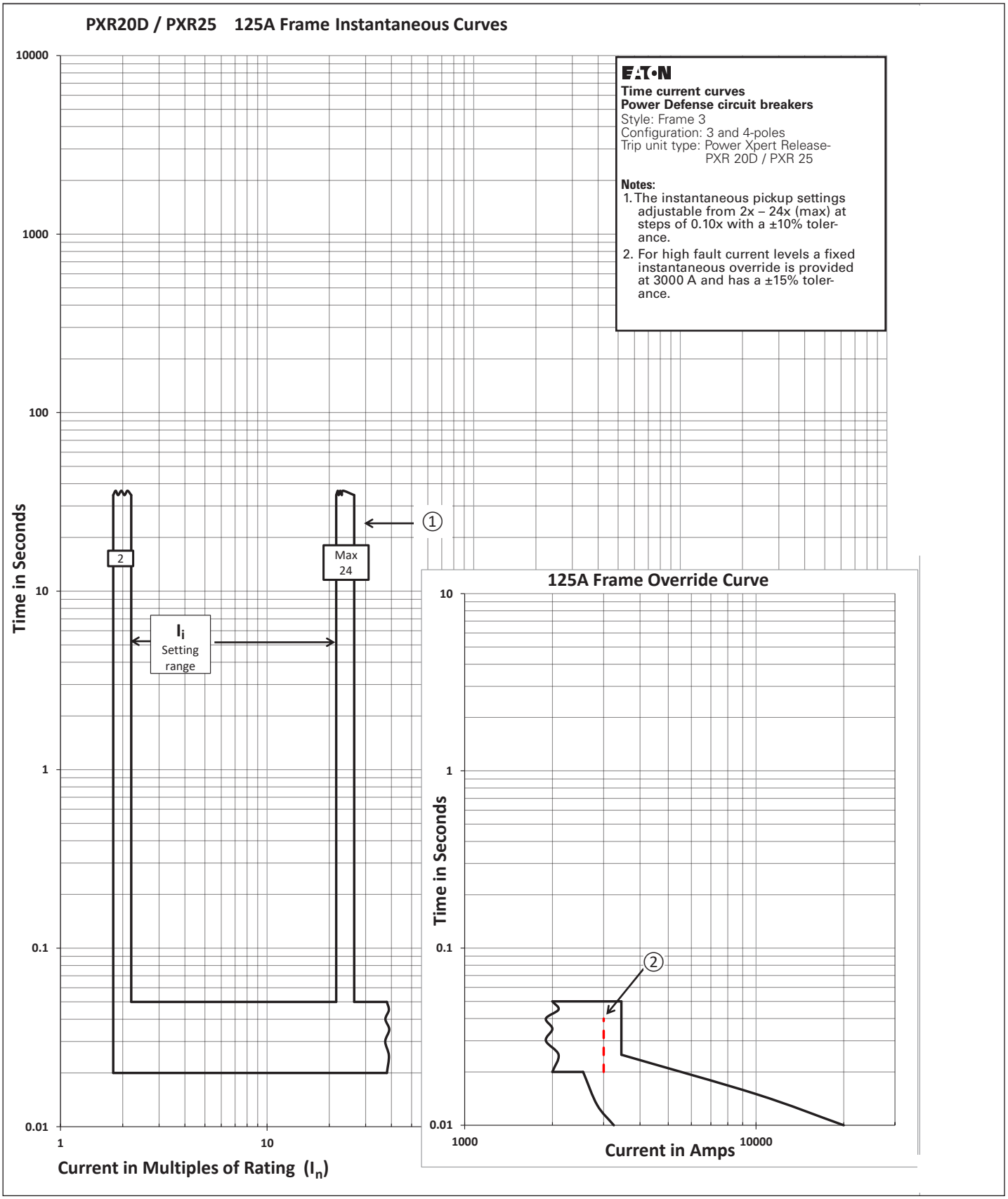

Figure 11. PXR 20D / PXR 25 - instantaneous and override for 125A frame.

January 2025

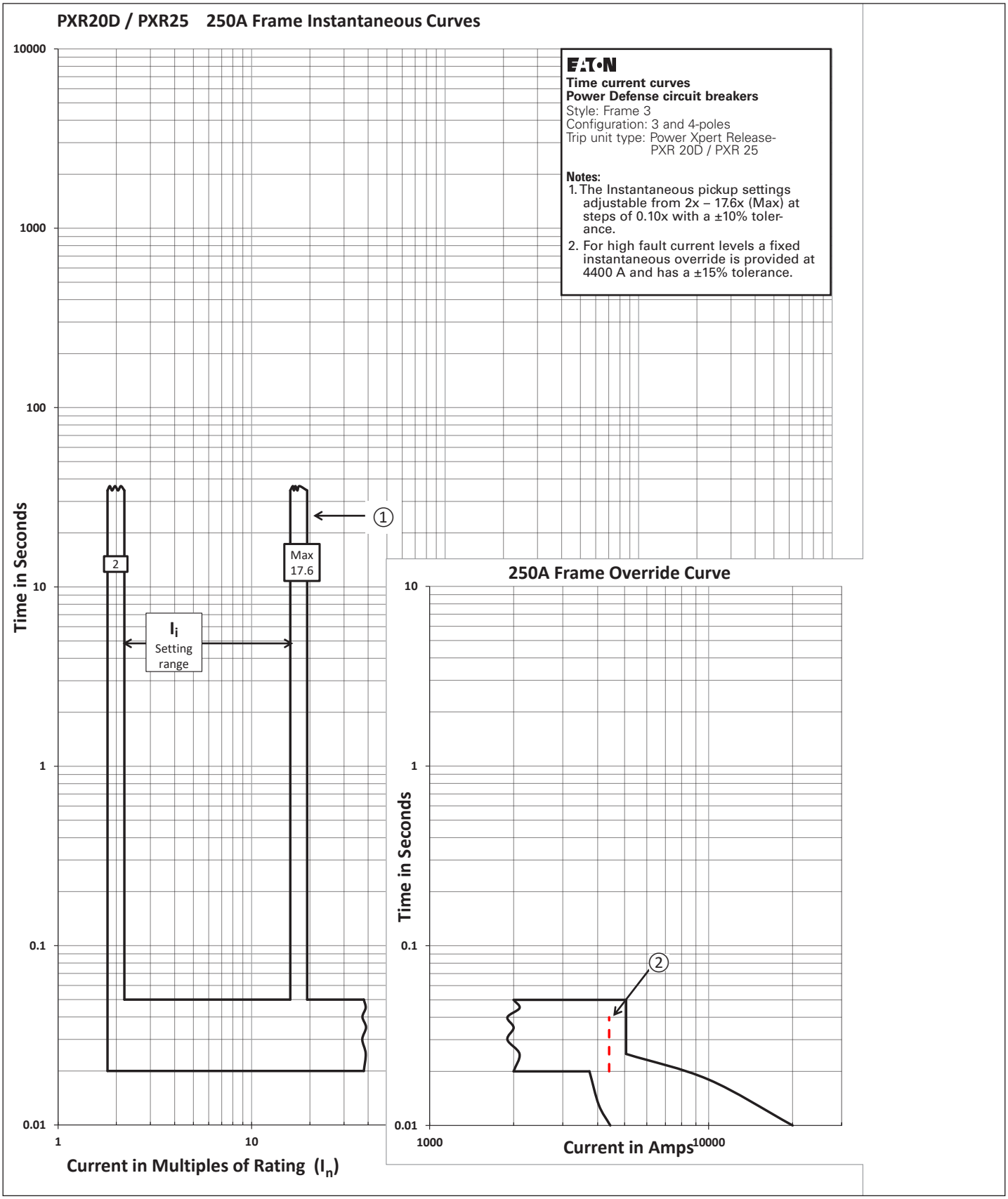

Figure 12. PXR 20D / PXR 25 - instantaneous and override for 250A frame. **January 2025**

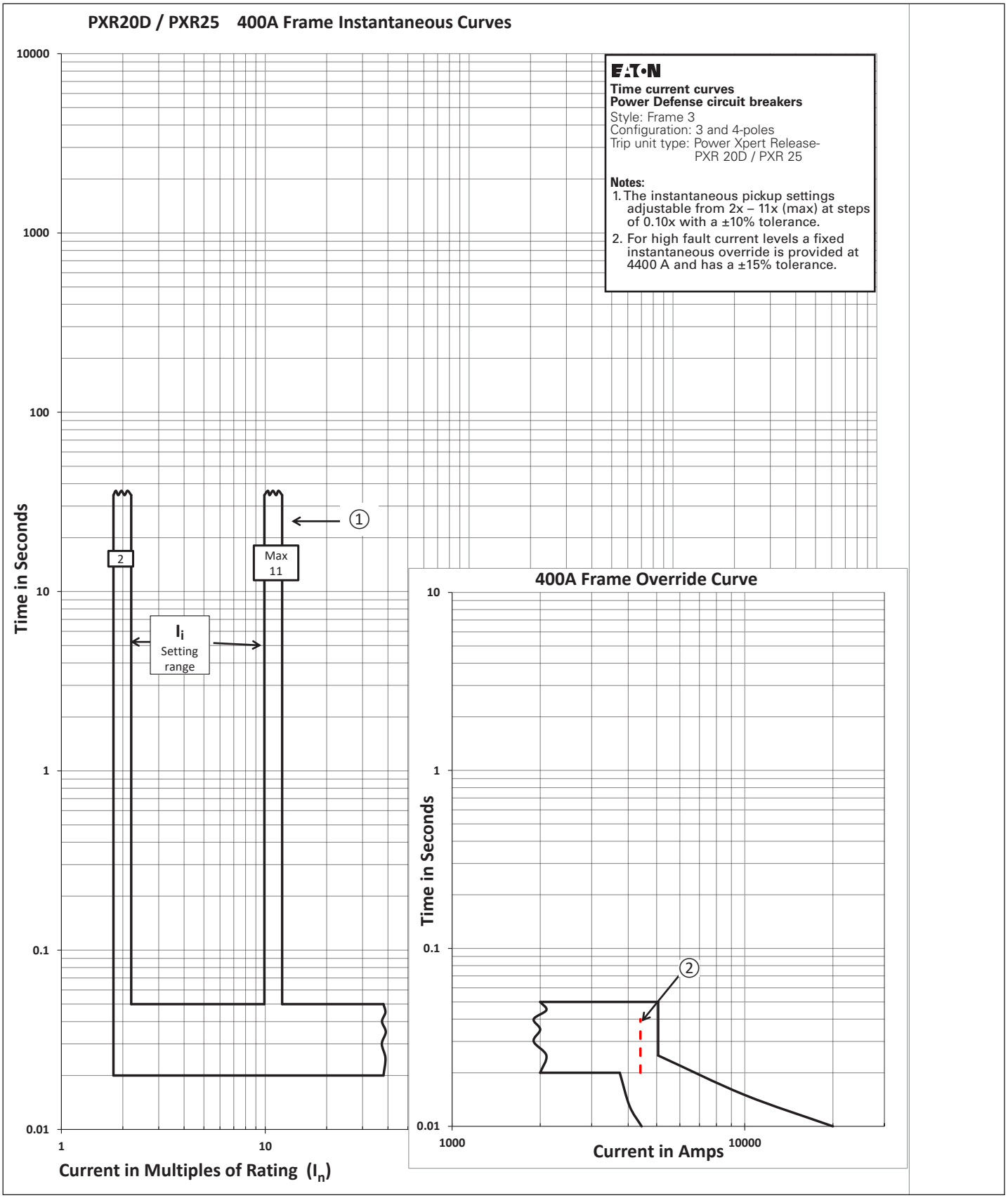

Figure 13. PXR 20D / PXR 25 - instantaneous and override for 400A frame.

January 2025

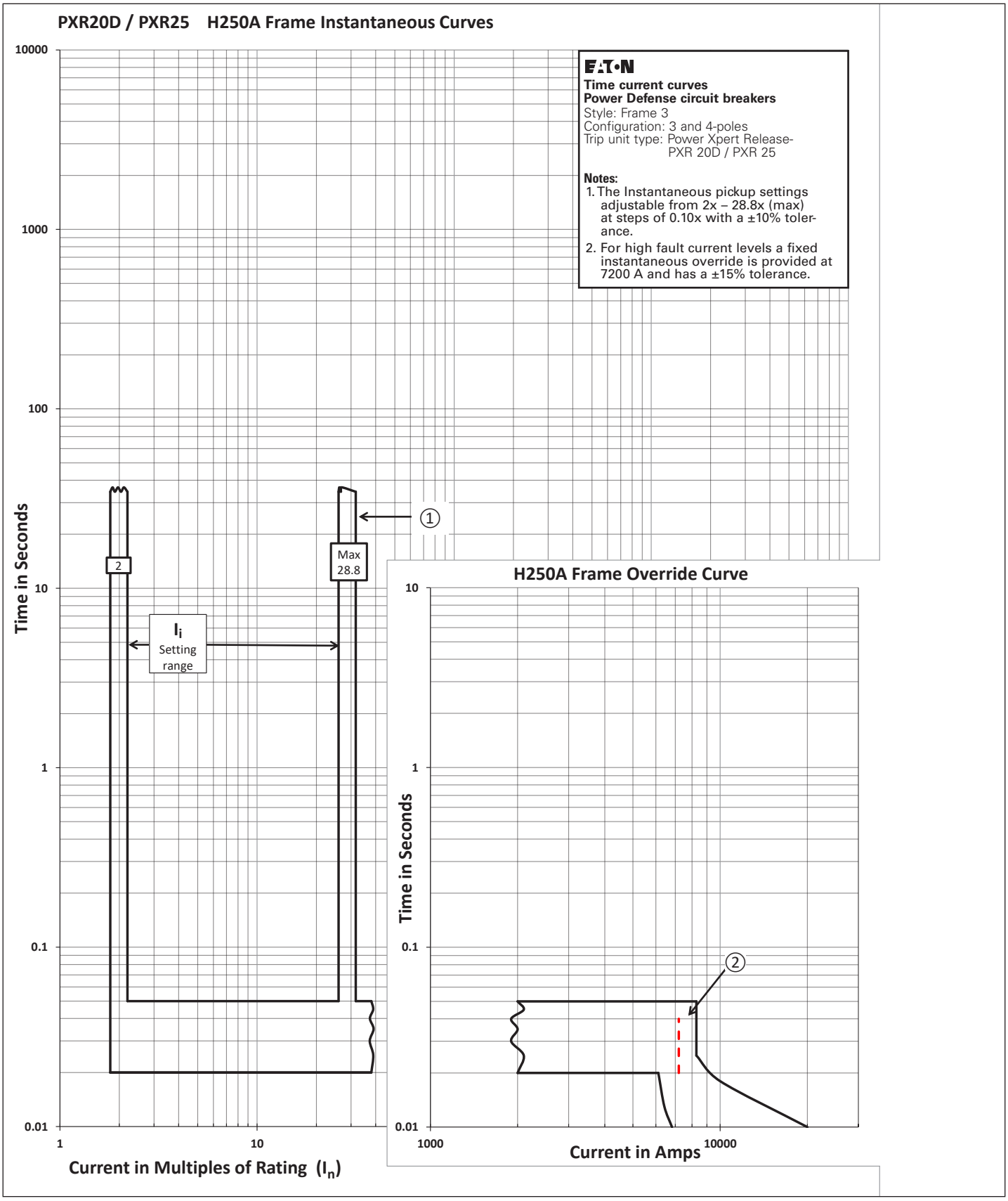

Figure 14. PXR 20D / PXR 25 - instantaneous and override for H250A frame. **January 2025**

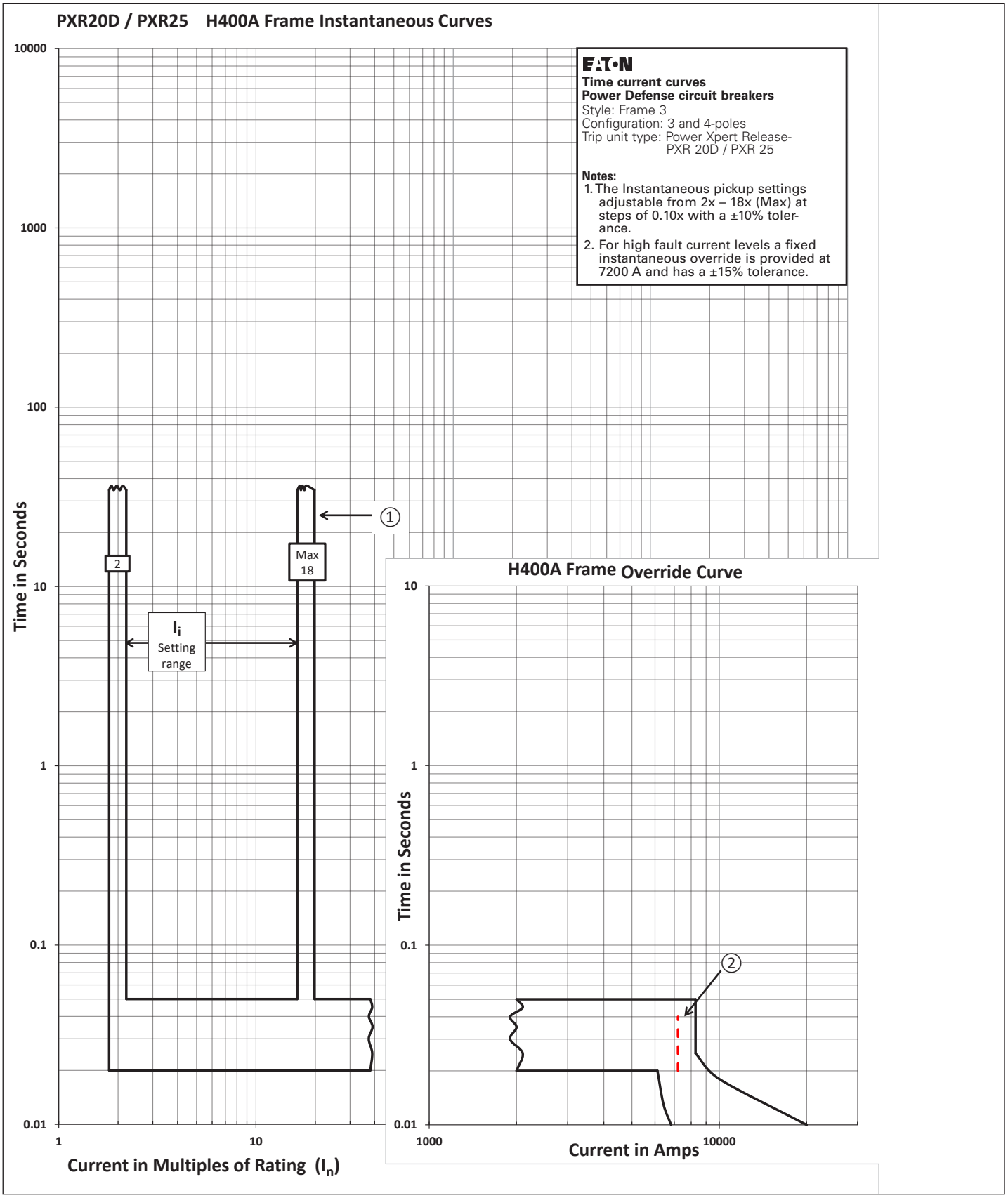

Figure 15. PXR 20D / PXR 25 - Instantaneous and override for H400A frame.

January 2025

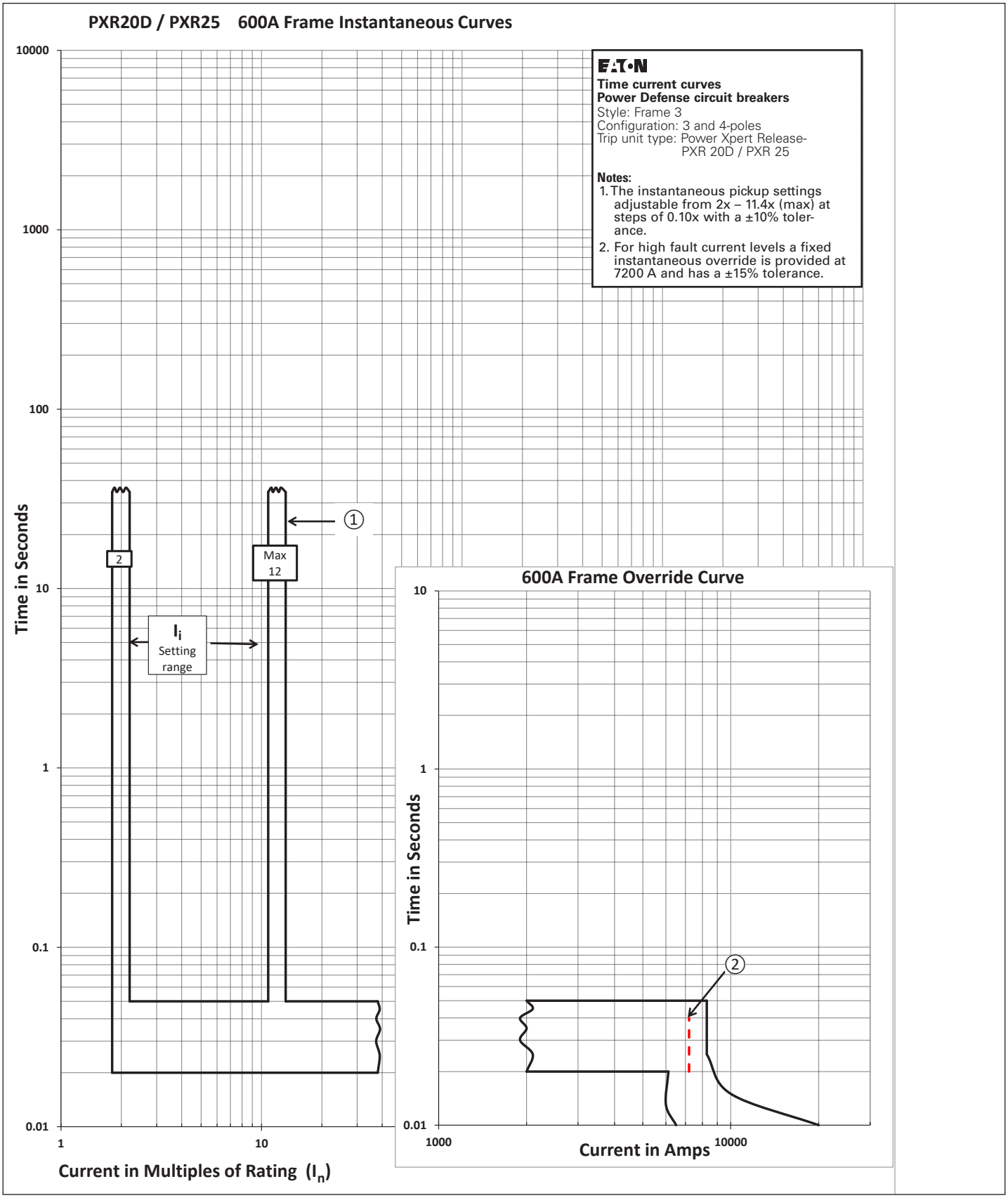

Figure 16. PXR 20D / PXR 25 - instantaneous and override for 600A frame. **January 2025**

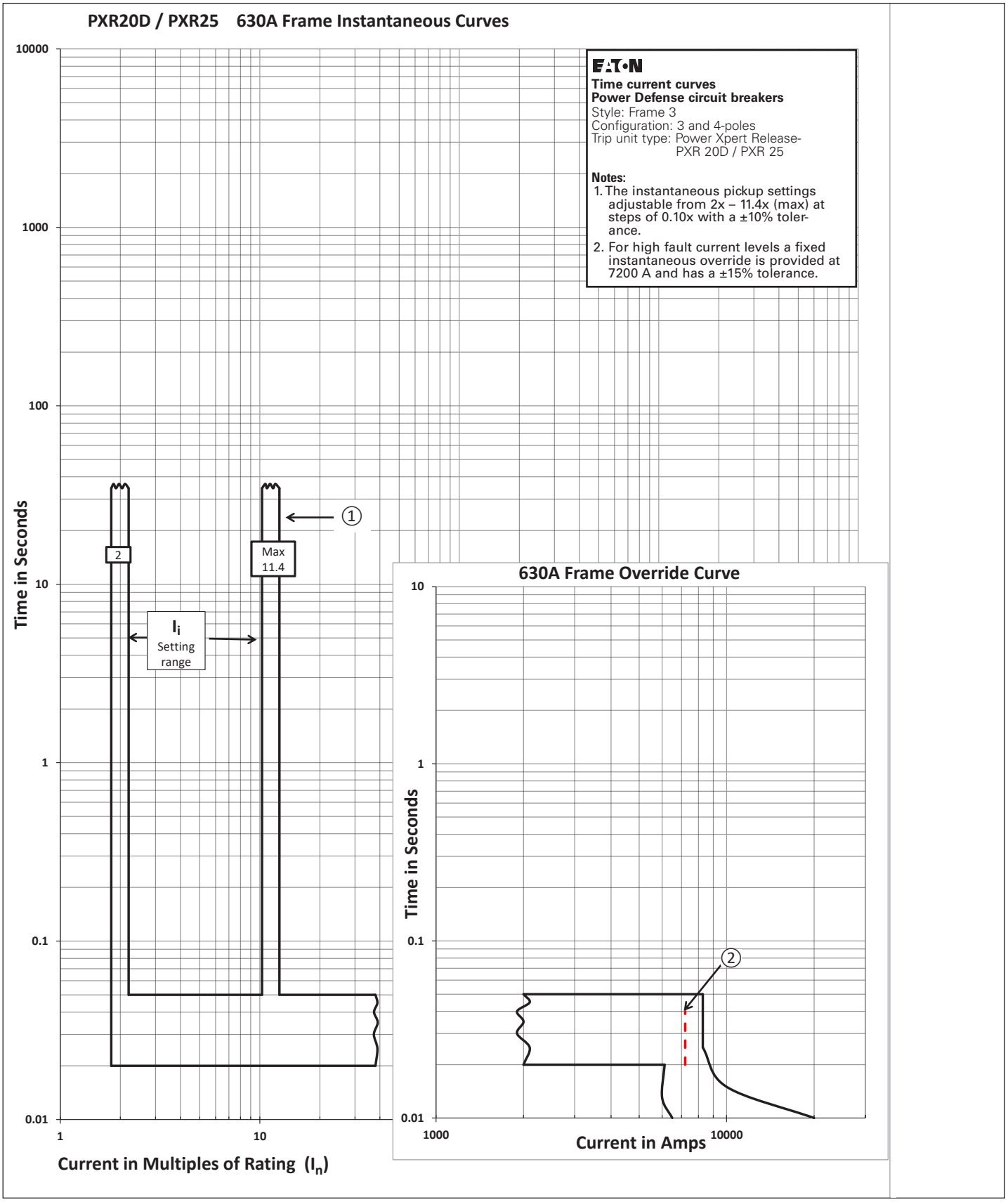

Figure 17. PXR 20D / PXR 25 -instantaneous and override for 630A frame.

January 2025

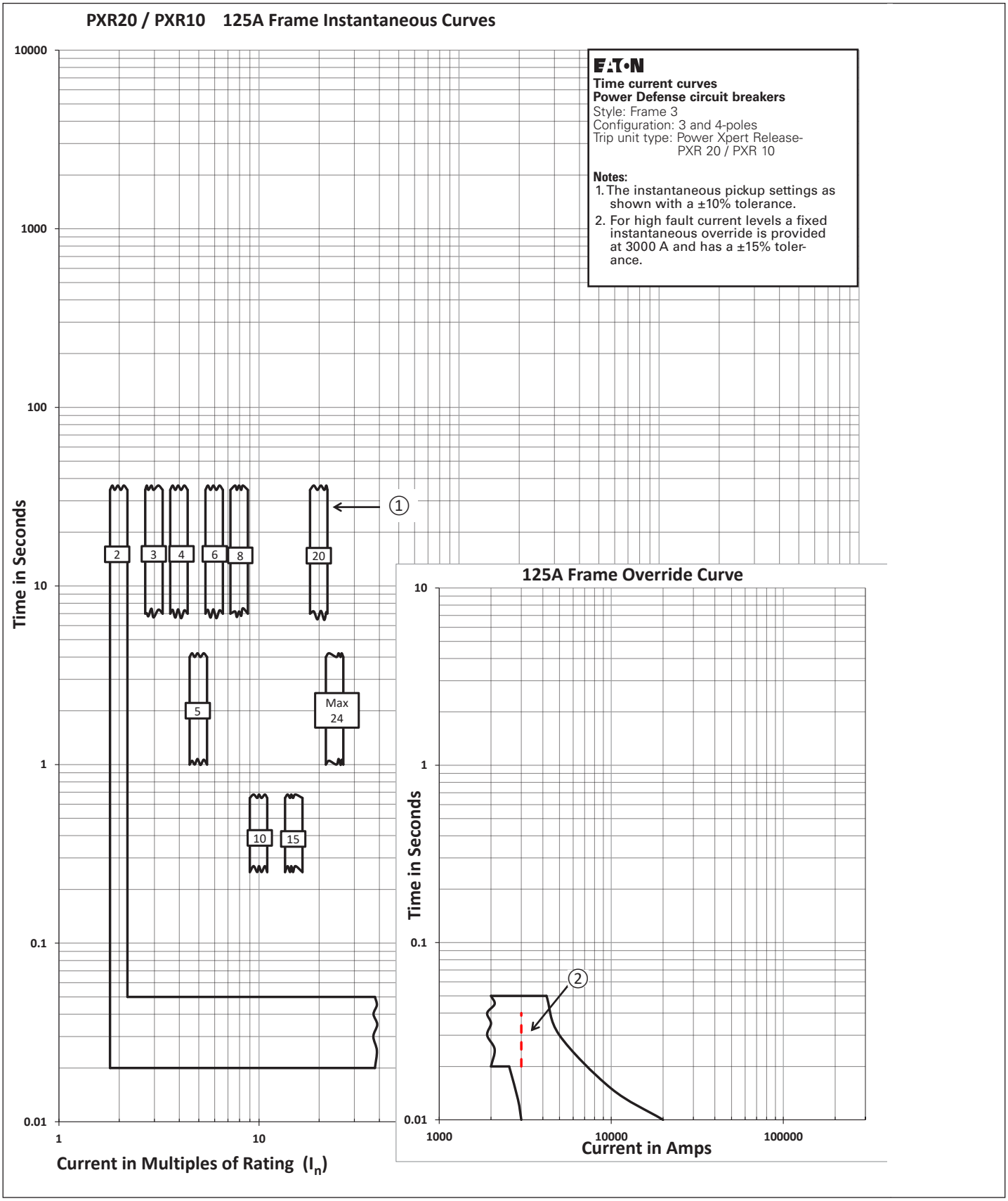

Figure 18. PXR 20 / PXR 10 - instantaneous and override for 125A frame. **January 2025**

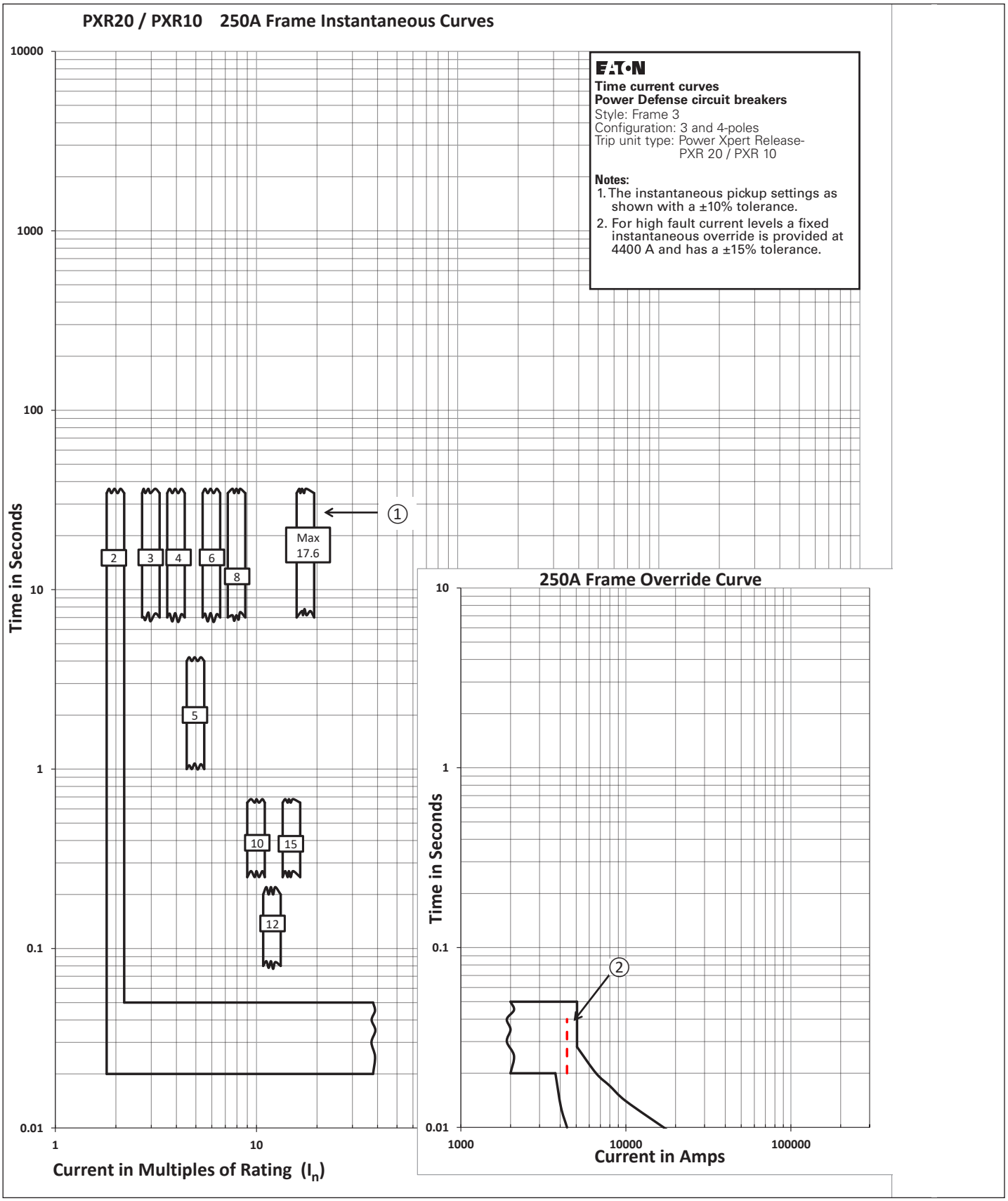

Figure 19. PXR 20 / PXR 10 - instantaneous and override for 250A frame.

January 2025

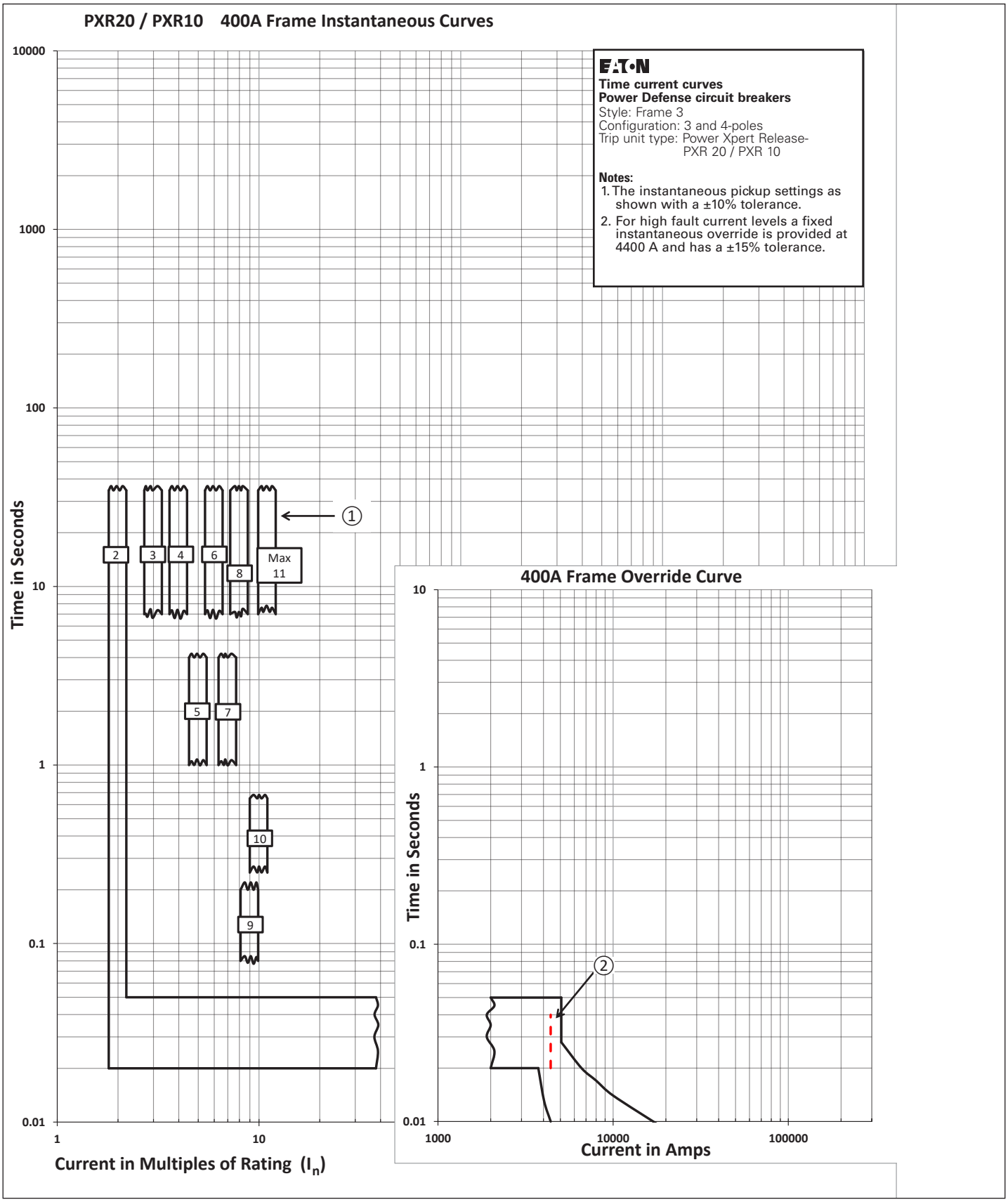

Figure 20. PXR 20 / PXR 10 - instantaneous and override for 400A frame.

January 2025

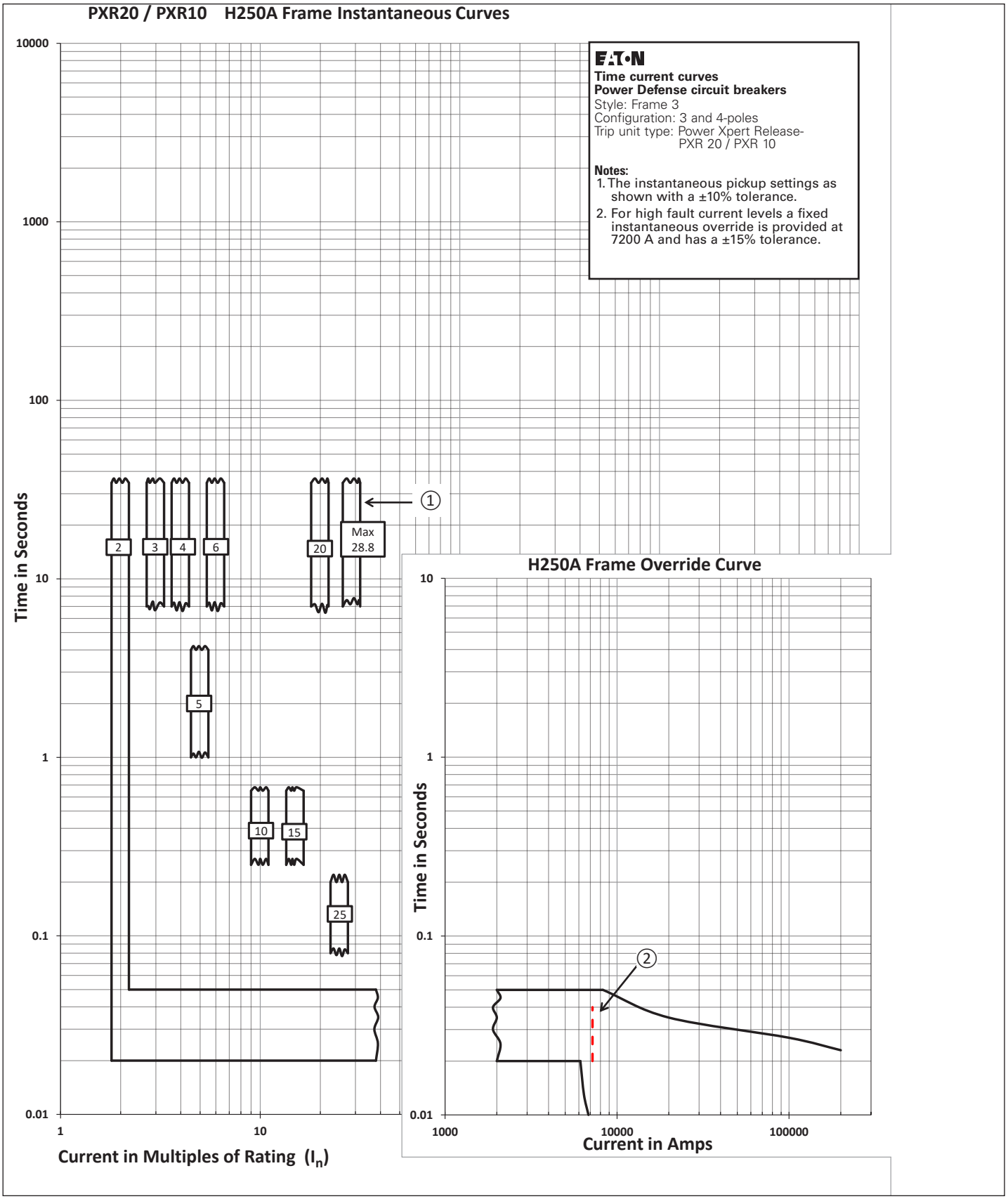

Figure 21. PXR 20 / PXR 10 - instantaneous and override for H250A frame.

January 2025

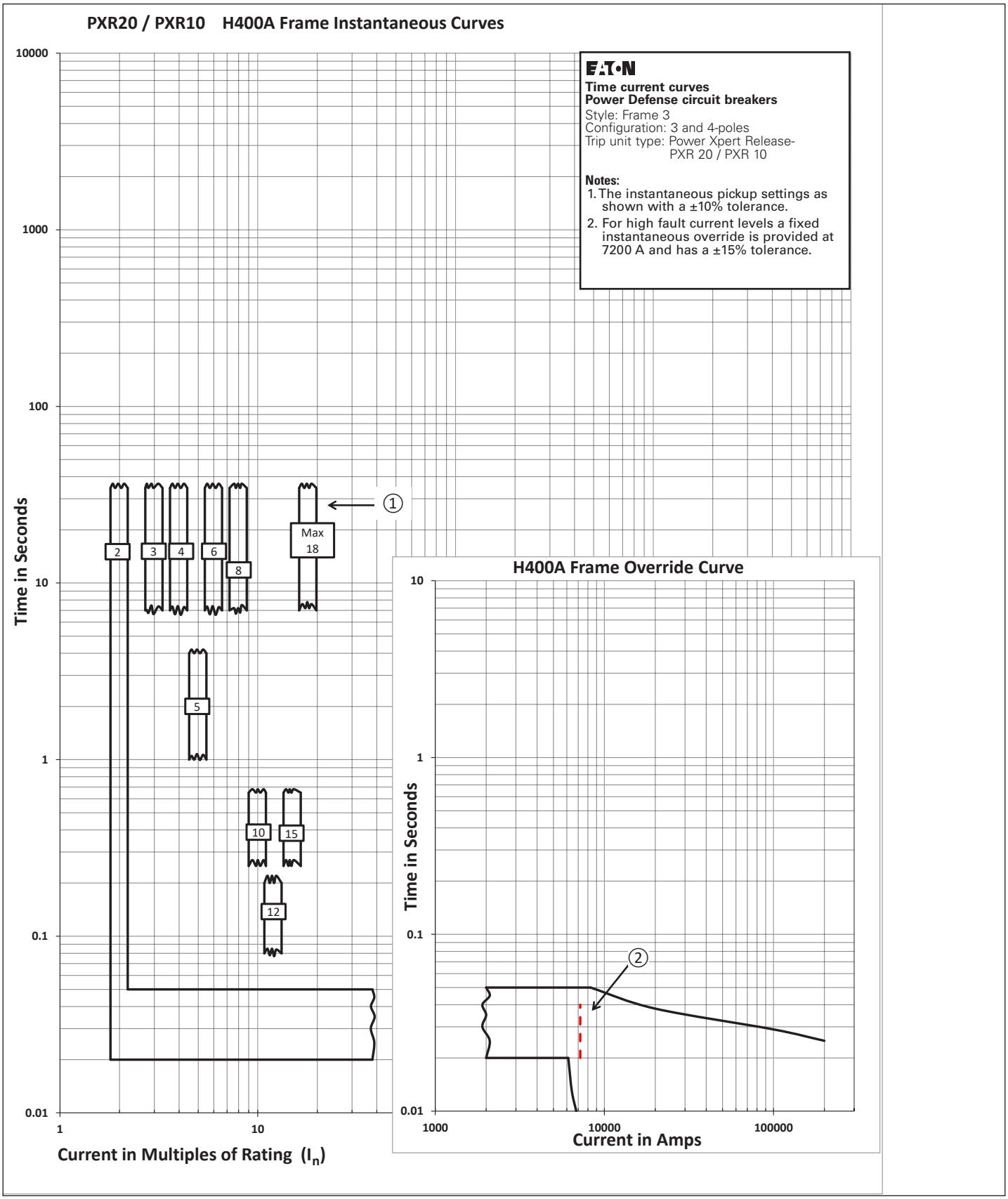

Figure 22. PXR 20 / PXR 10 - instantaneous and override for H400A frame.

January 2025

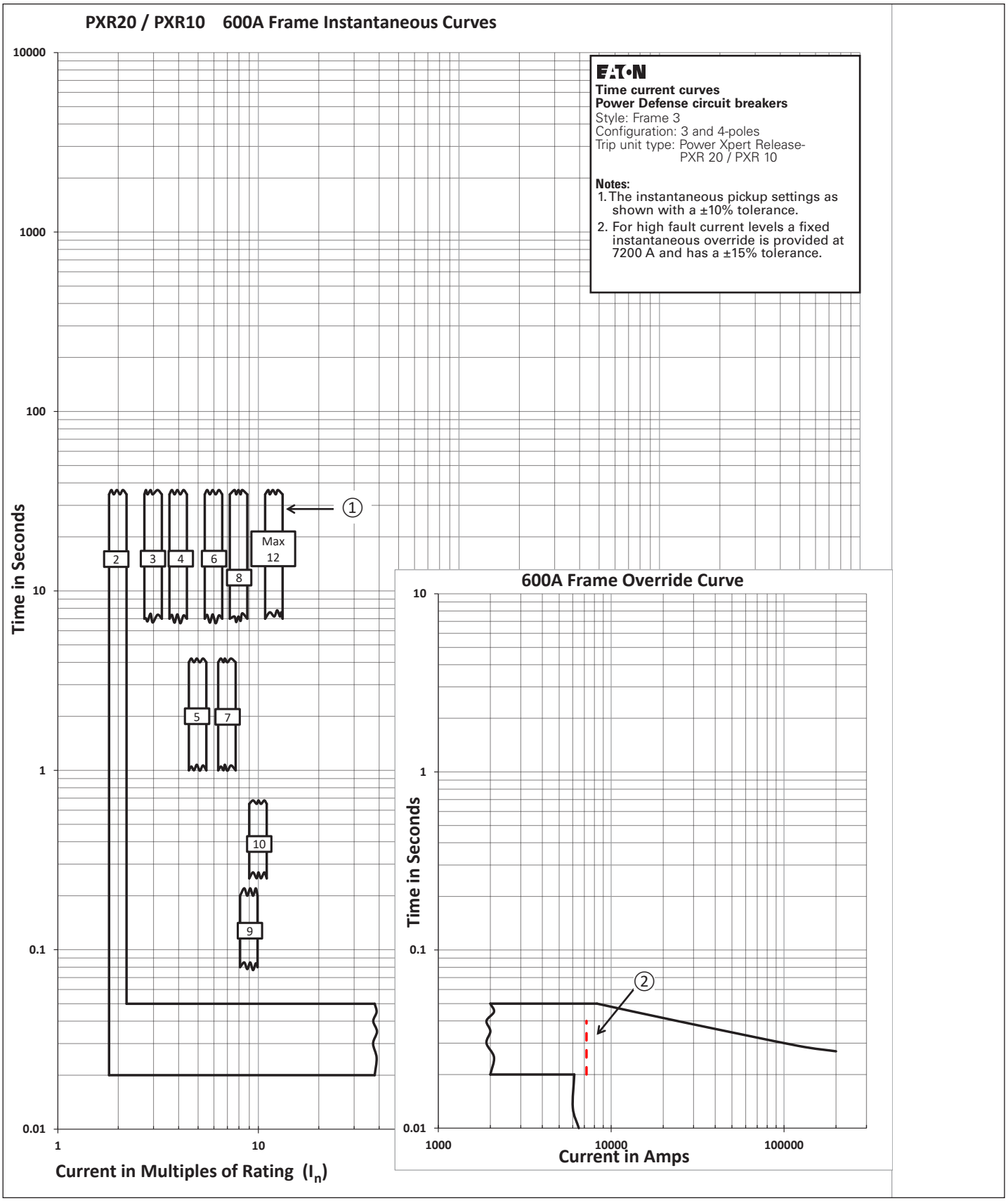

Figure 23. PXR 20 / PXR 10 - instantaneous and override for 600A frame.

January 2025

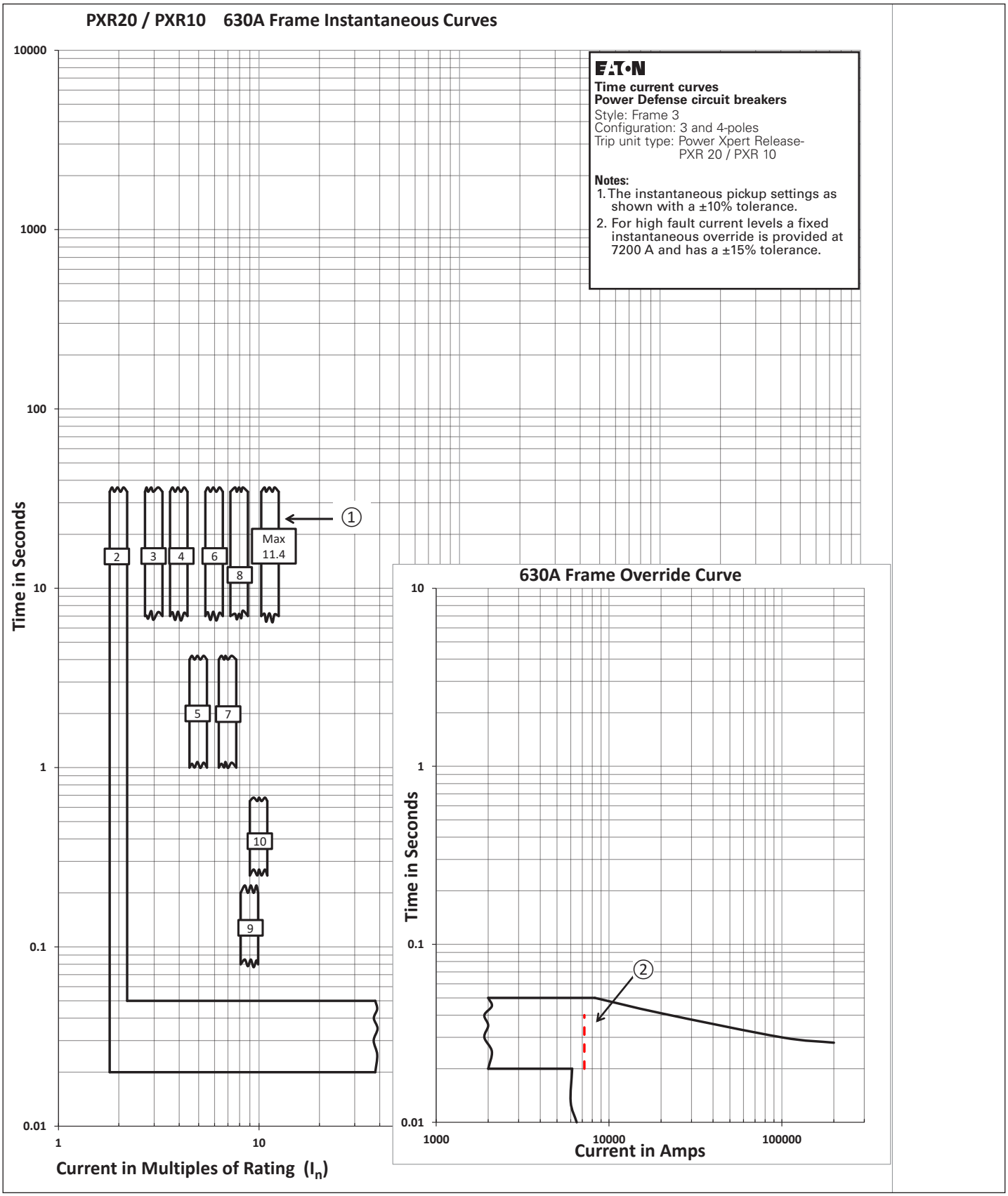

Figure 24. PXR 20 / PXR 10 - instantaneous and override for 630A frame.

January 2025

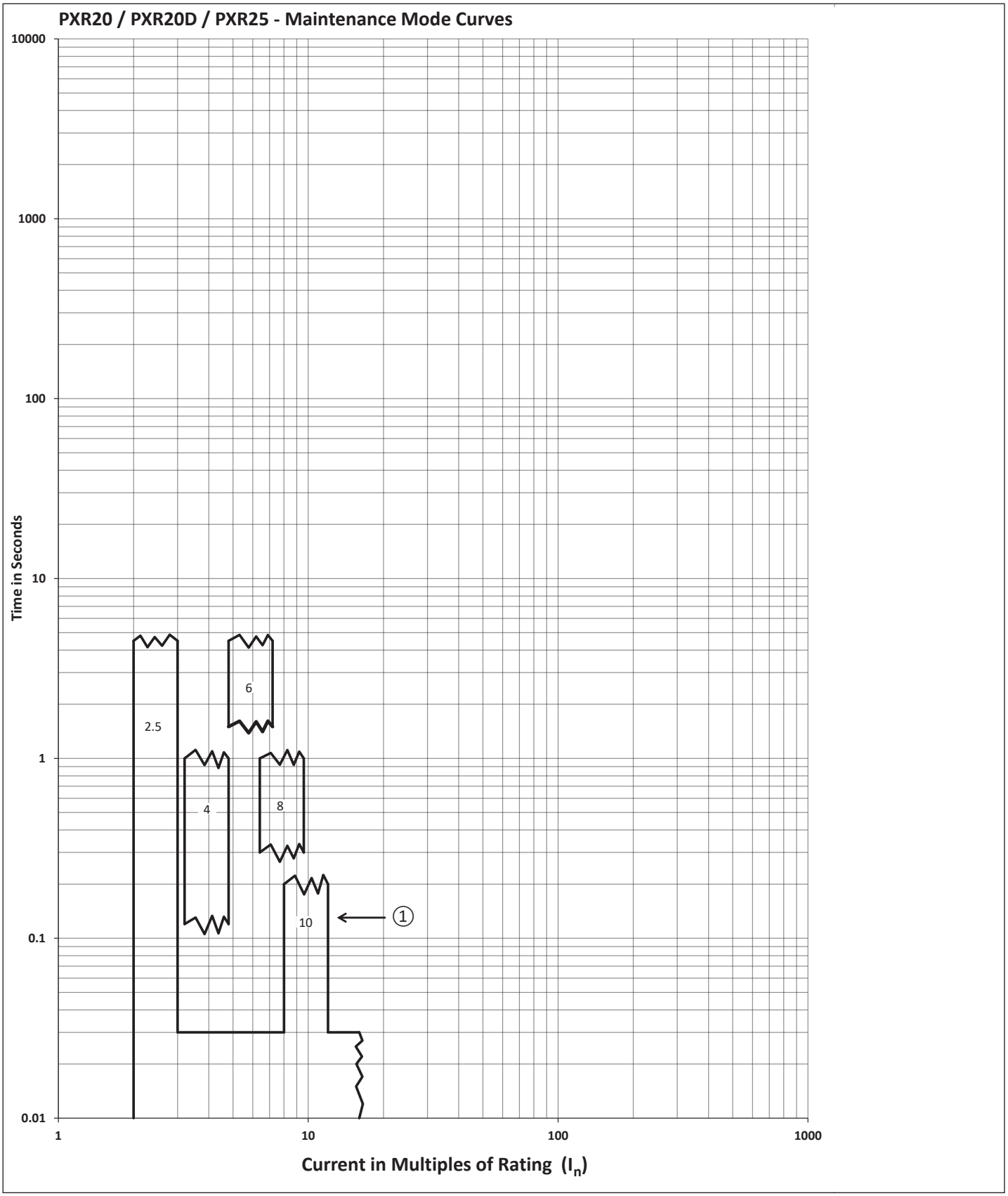

Figure 25. PXR 20 / PXR 20D / PXR 25 - maintenance mode.

January 2025

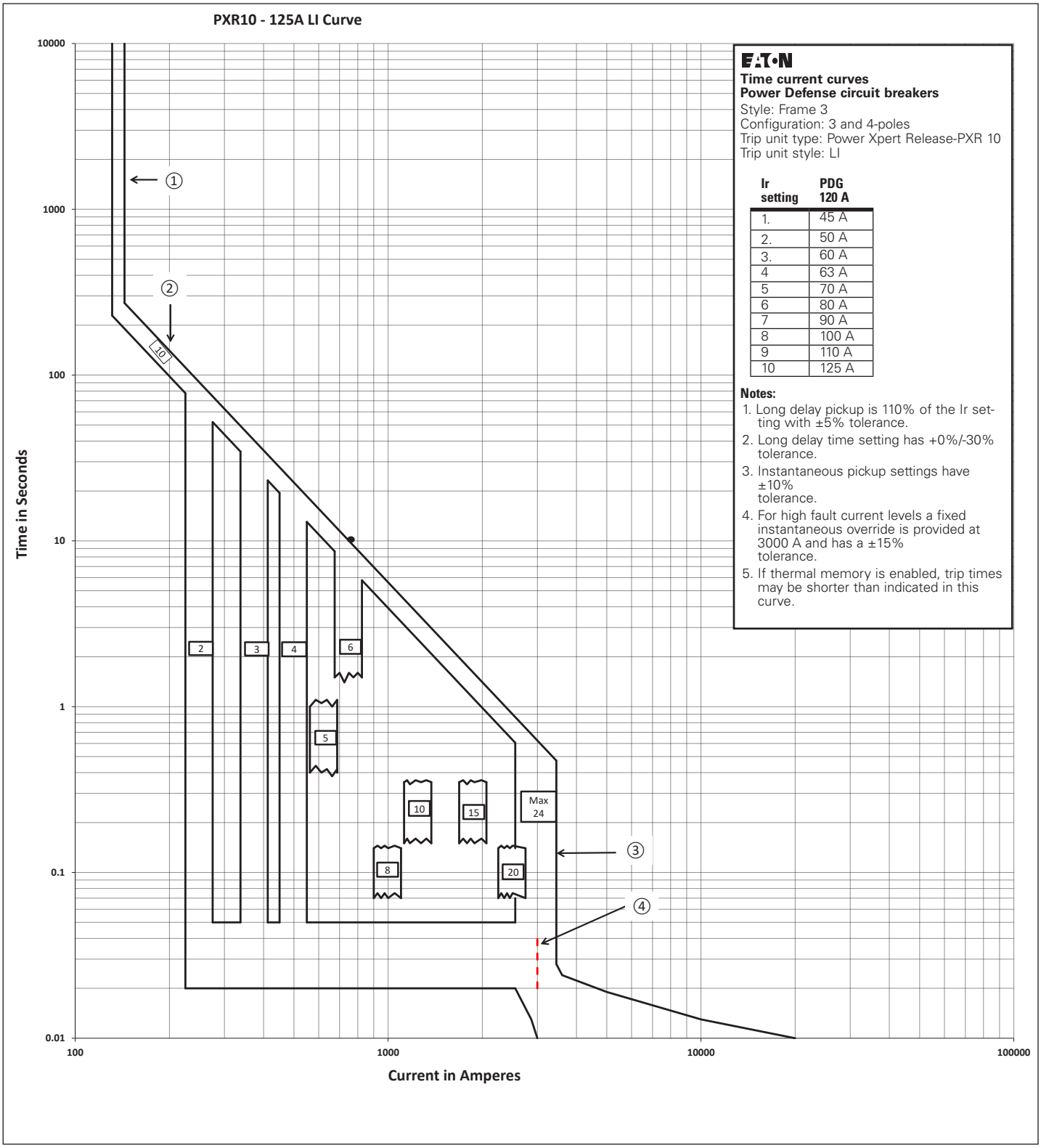

Figure 26. PXR 10 LI 125A frame.

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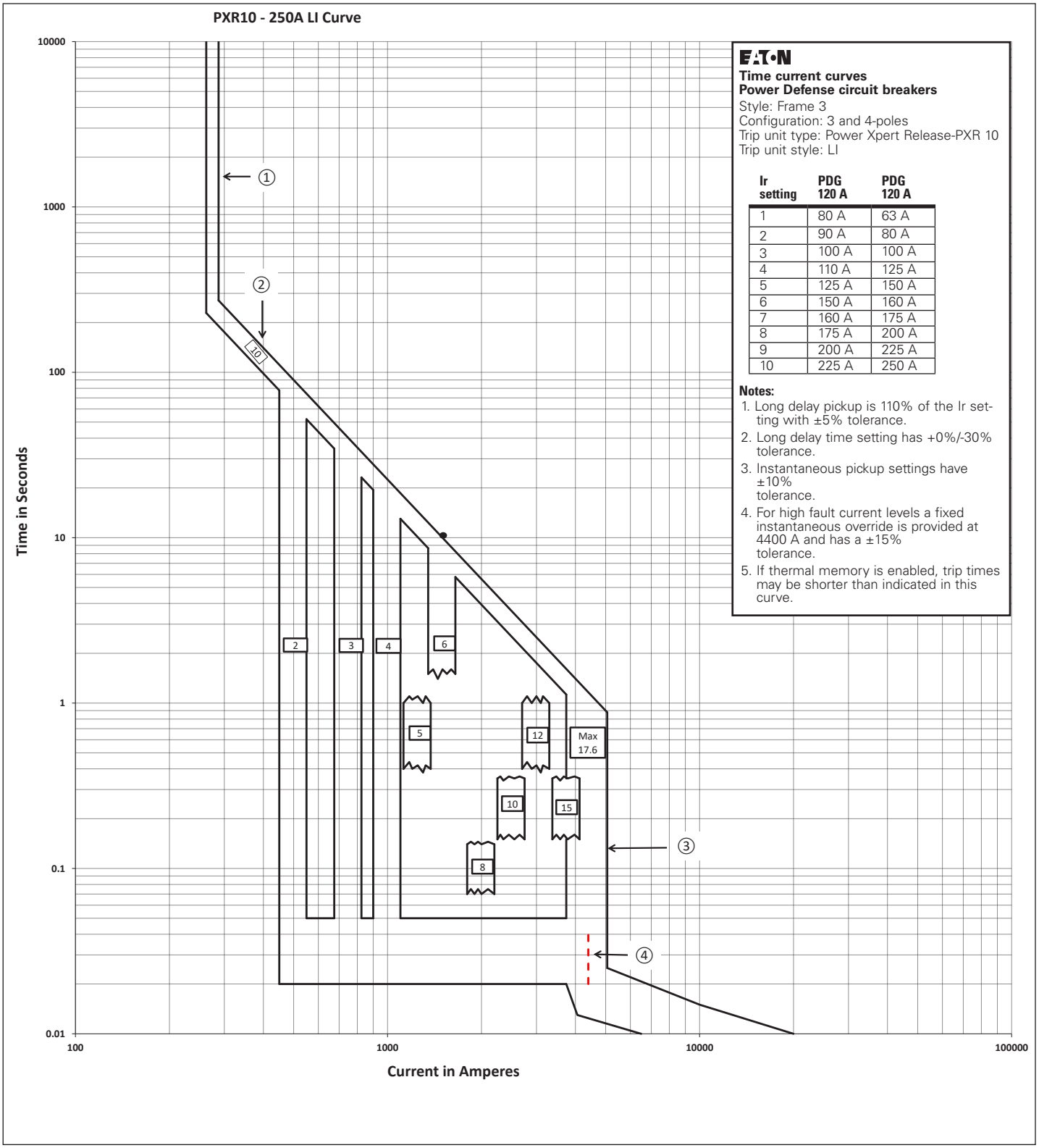
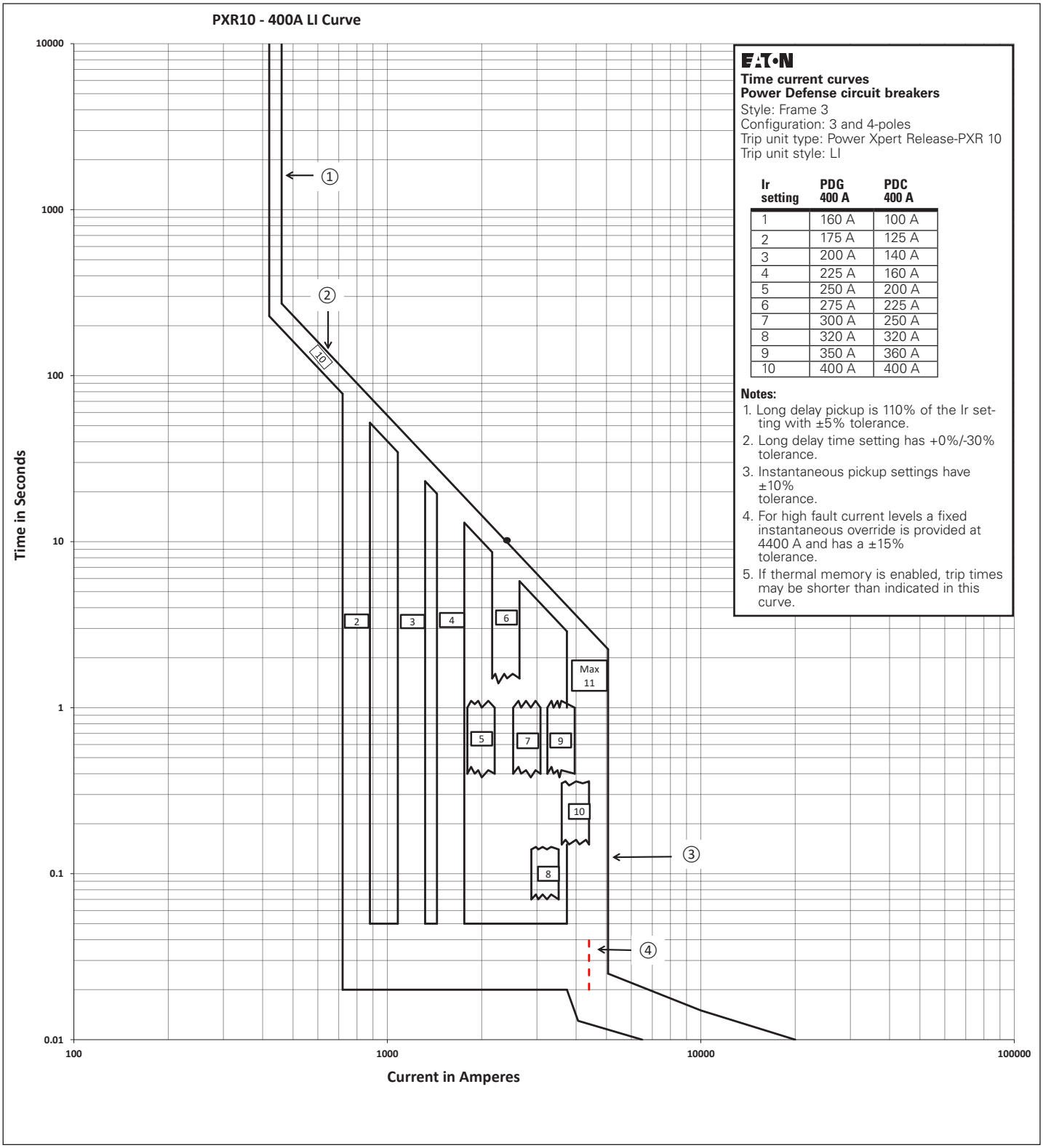


Figure 27. PXR 10 LI 250A frame.

January 2025



Ir setting	PDG 400 A	PDC 400 A
1	160 A	100 A
2	175 A	125 A
3	200 A	140 A
4	225 A	160 A
5	250 A	200 A
6	275 A	225 A
7	300 A	250 A
8	320 A	320 A
9	350 A	360 A
10	400 A	400 A

Figure 28. PXR 10 LI 400A frame.

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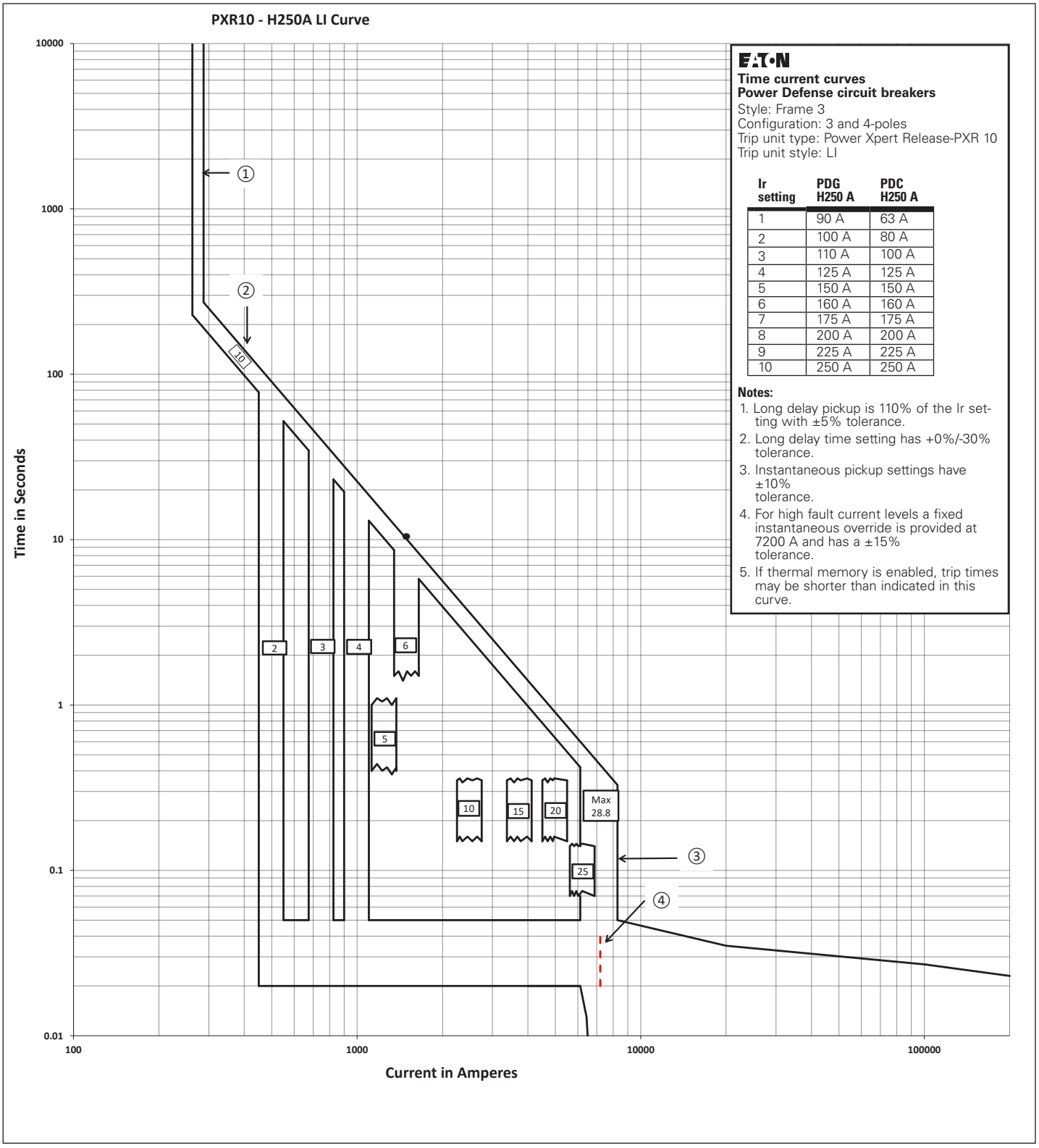

Time current curves
Power Defense circuit breakers

Style: Frame 3
Configuration: 3 and 4-poles
Trip unit type: Power Xpert Release-PXR 10
Trip unit style: LI

Ir setting	PDG H250 A	PDC H250 A
1	90 A	63 A
2	100 A	80 A
3	110 A	100 A
4	125 A	125 A
5	150 A	150 A
6	160 A	160 A
7	175 A	175 A
8	200 A	200 A
9	225 A	225 A
10	250 A	250 A

Notes:

1. Long delay pickup is 110% of the Ir setting with ±5% tolerance.
2. Long delay time setting has +0%/-30% tolerance.
3. Instantaneous pickup settings have ±10% tolerance.
4. For high fault current levels a fixed instantaneous override is provided at 7200 A and has a ±15% tolerance.
5. If thermal memory is enabled, trip times may be shorter than indicated in this curve.

Figure 29. PXR 10 LI H250A frame.

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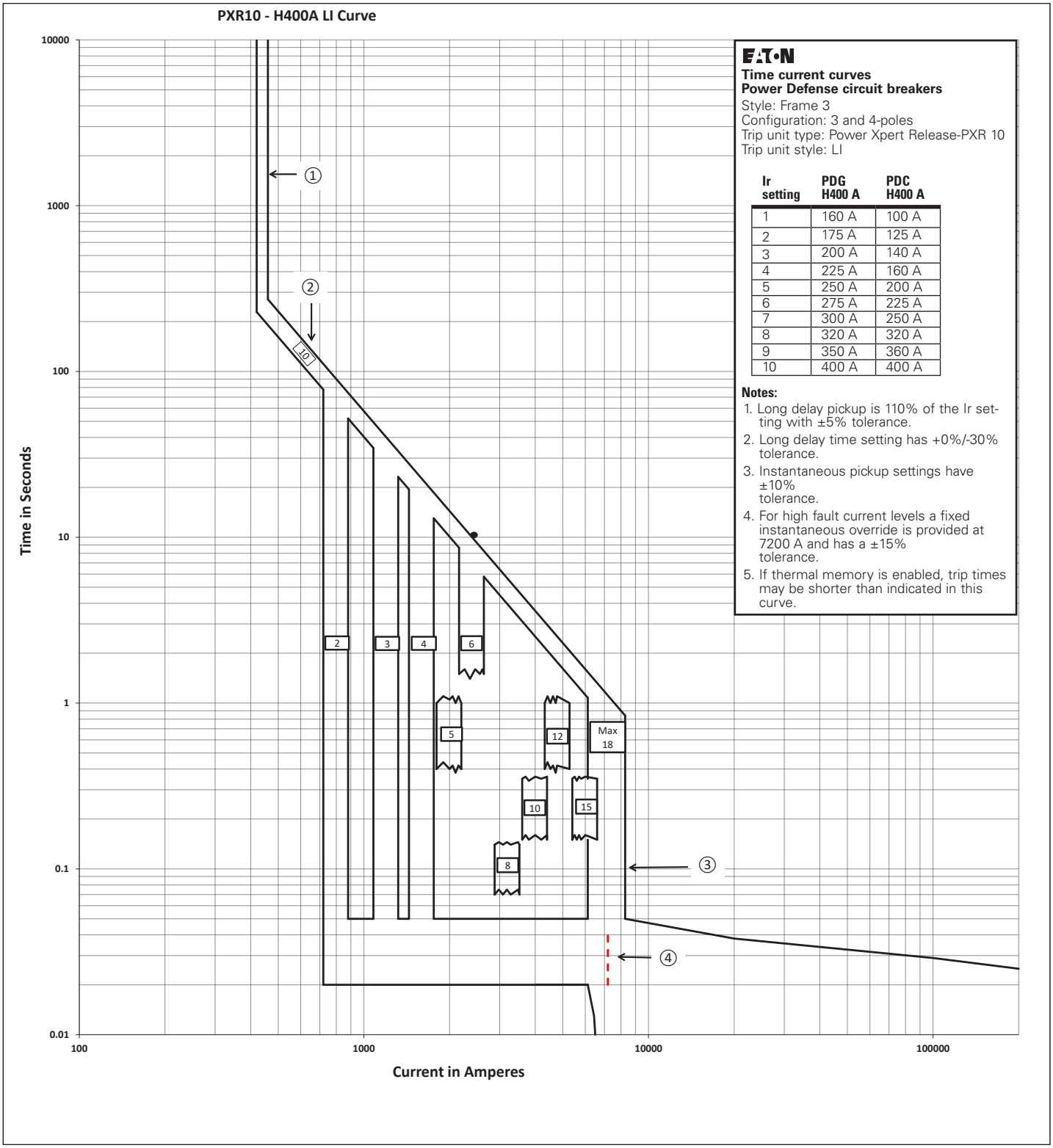

Figure 30. PXR 10 LI H400A frame.

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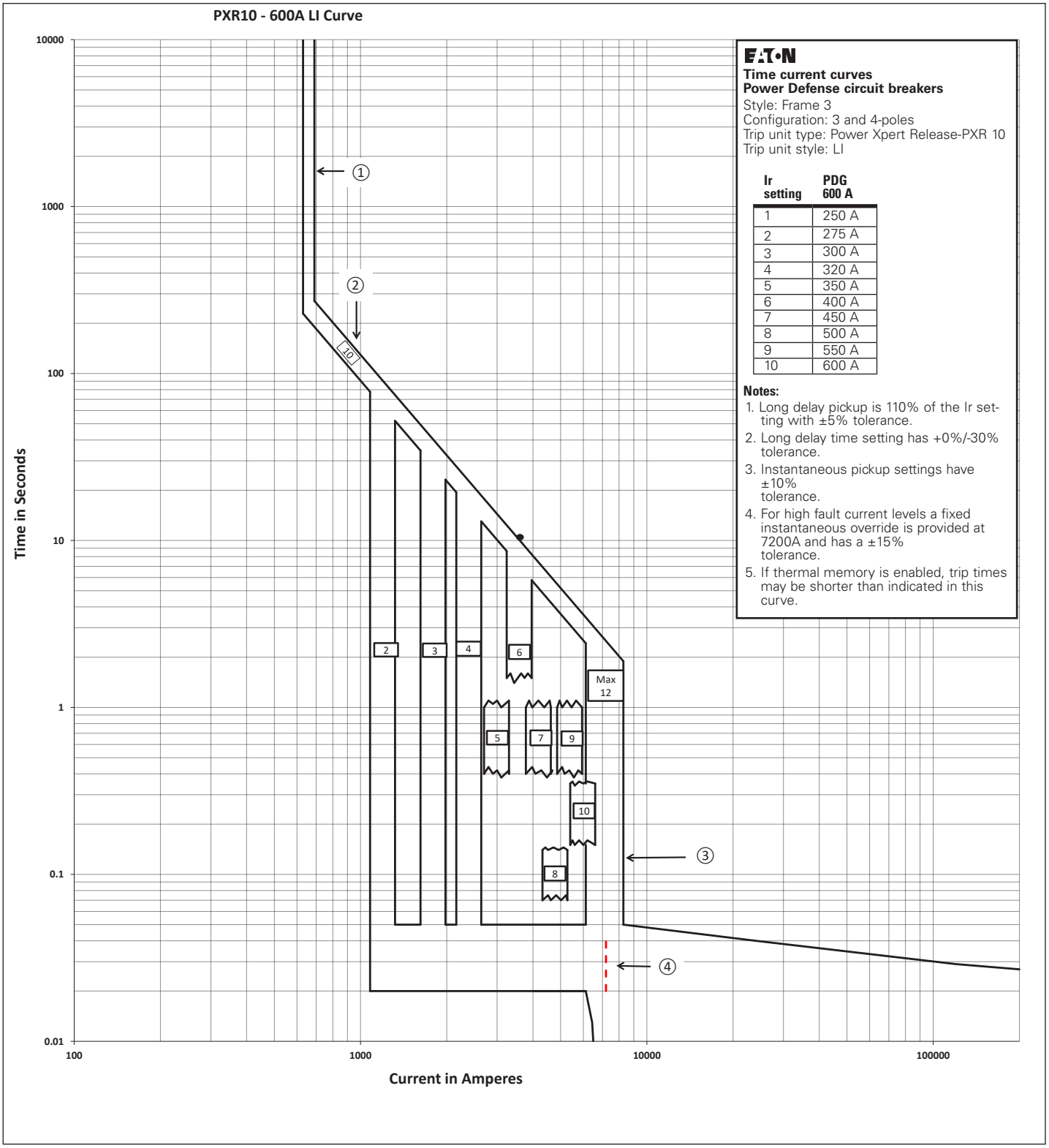

Figure 31. PXR 10 LI 600A frame.

January 2025

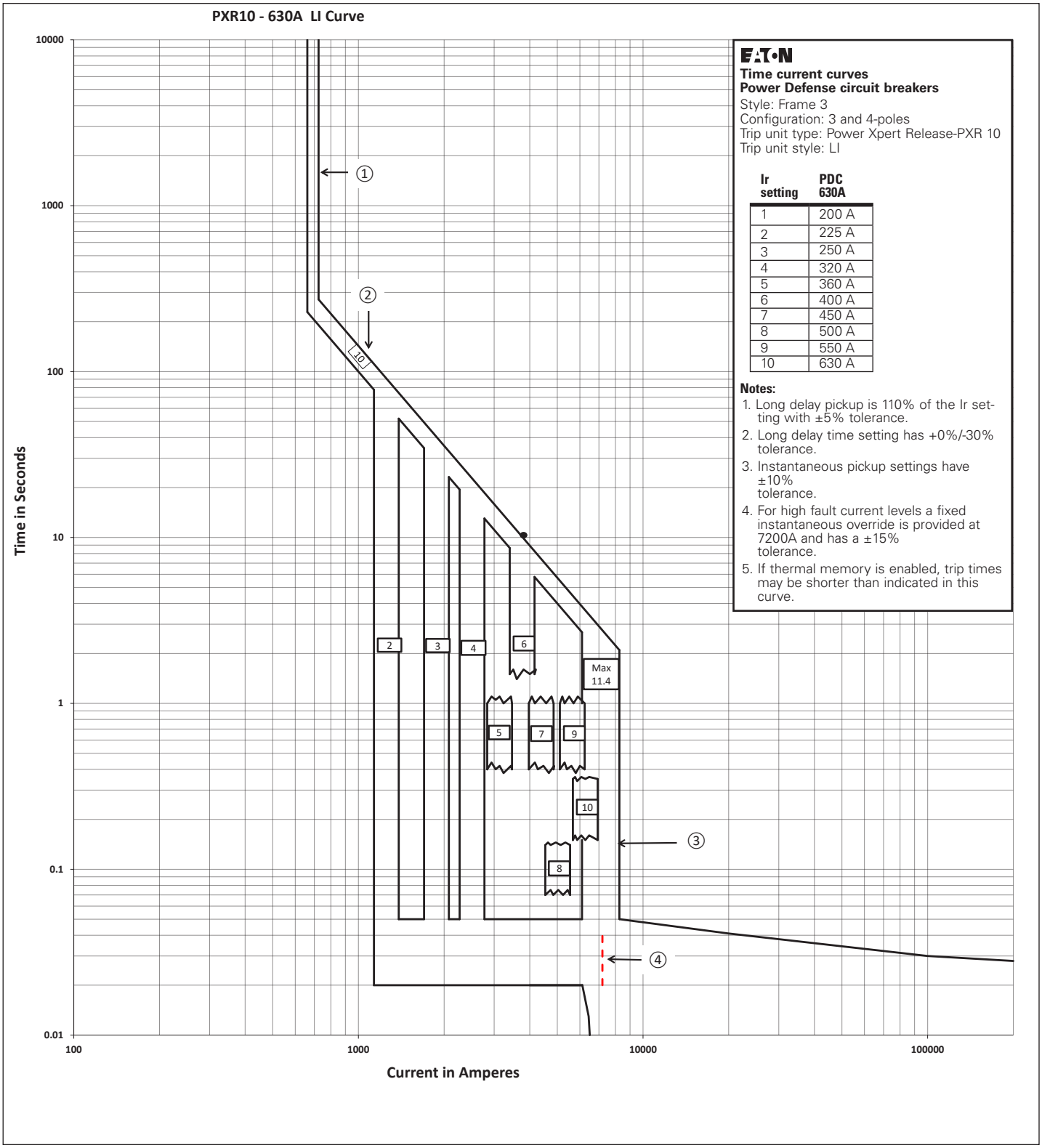

Figure 32. PXR 10 LI 630A frame.

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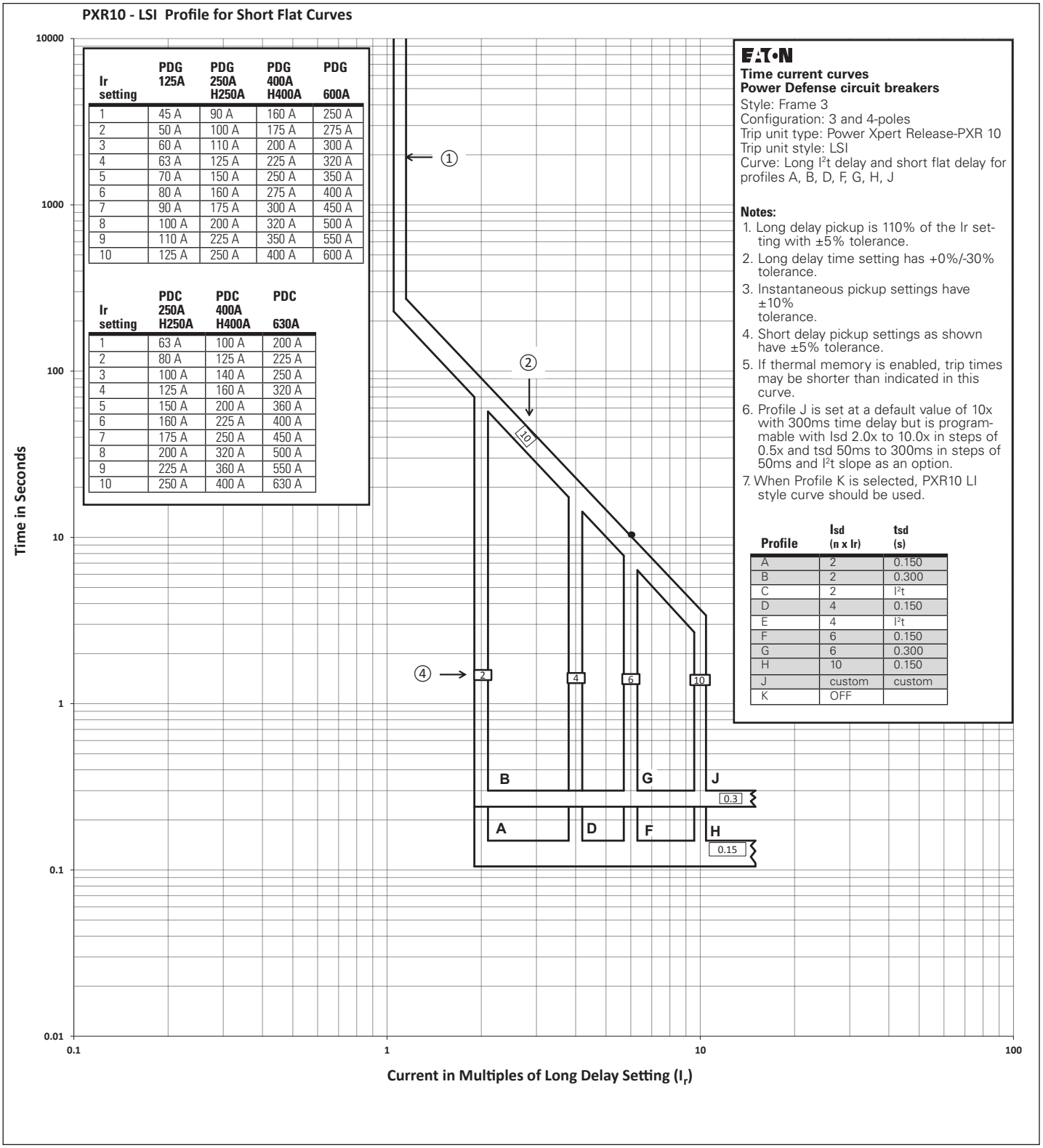

Ir setting	PDG 125A	PDG 250A H250A	PDG 400A H400A	PDG 600A
1	45 A	90 A	160 A	250 A
2	50 A	100 A	175 A	275 A
3	60 A	110 A	200 A	300 A
4	63 A	125 A	225 A	320 A
5	70 A	150 A	250 A	350 A
6	80 A	160 A	275 A	400 A
7	90 A	175 A	300 A	450 A
8	100 A	200 A	320 A	500 A
9	110 A	225 A	350 A	550 A
10	125 A	250 A	400 A	600 A

Ir setting	PDC 250A H250A	PDC 400A H400A	PDC 630A
1	63 A	100 A	200 A
2	80 A	125 A	225 A
3	100 A	140 A	250 A
4	125 A	160 A	320 A
5	150 A	200 A	360 A
6	160 A	225 A	400 A
7	175 A	250 A	450 A
8	200 A	320 A	500 A
9	225 A	360 A	550 A
10	250 A	400 A	630 A

EATON

Time current curves
Power Defense circuit breakers

Style: Frame 3
Configuration: 3 and 4-poles
Trip unit type: Power Xpert Release-PXR 10
Trip unit style: LSI
Curve: Long I^2t delay and short flat delay for profiles A, B, D, F, G, H, J

Notes:

1. Long delay pickup is 110% of the Ir setting with ±5% tolerance.
2. Long delay time setting has +0%/-30% tolerance.
3. Instantaneous pickup settings have ±10% tolerance.
4. Short delay pickup settings as shown have ±5% tolerance.
5. If thermal memory is enabled, trip times may be shorter than indicated in this curve.
6. Profile J is set at a default value of 10x with 300ms time delay but is programmable with Isd 2.0x to 10.0x in steps of 0.5x and tsd 50ms to 300ms in steps of 50ms and I^2t slope as an option.
7. When Profile K is selected, PXR10 LI style curve should be used.

Profile	Isd (n x Ir)	tsd (s)
A	2	0.150
B	2	0.300
C	2	I^2t
D	4	0.150
E	4	I^2t
F	6	0.150
G	6	0.300
H	10	0.150
J	custom	custom
K	OFF	

Figure 33. PXR 10 LSI profile for short flat curves.

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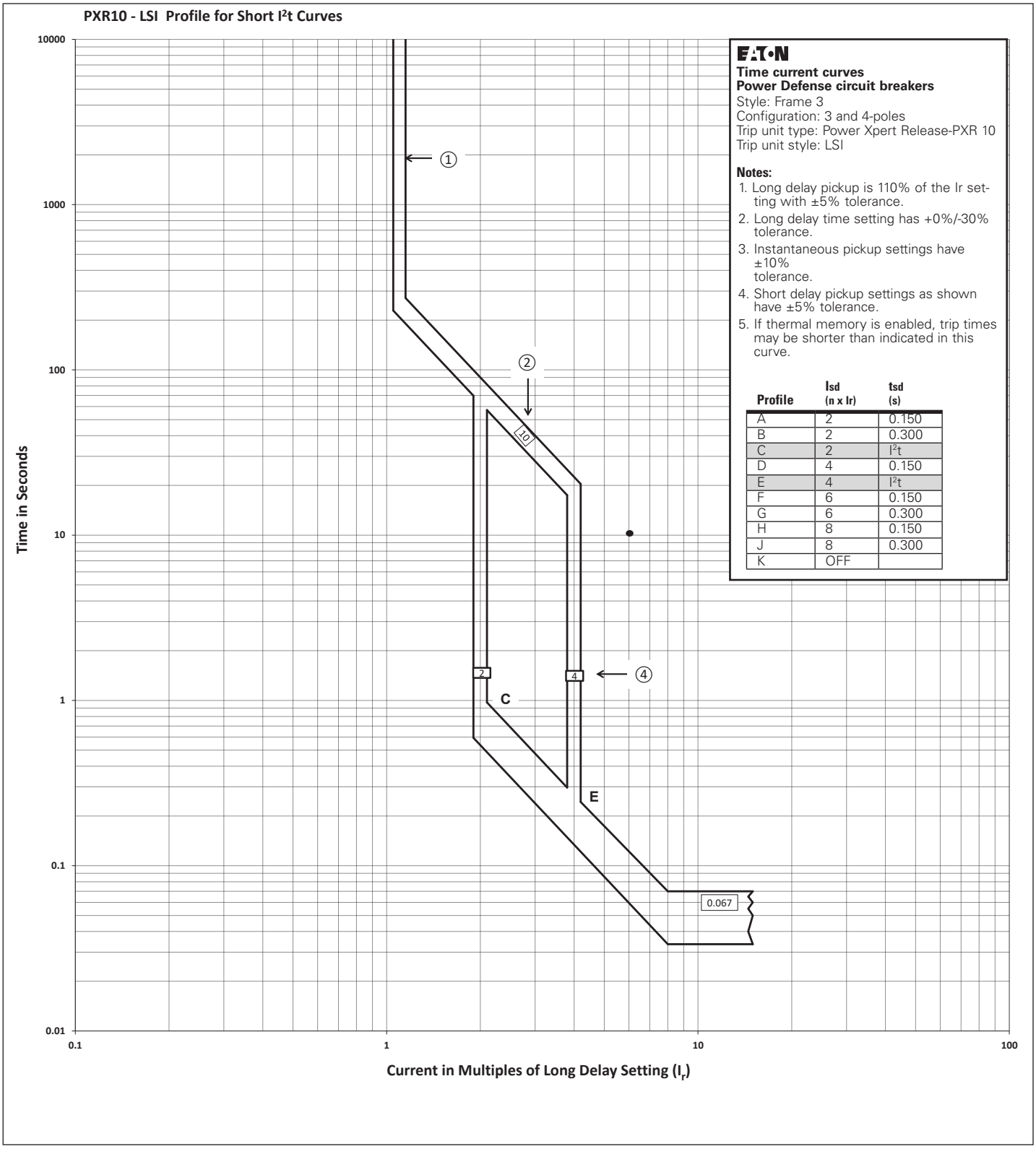

Figure 34. PXR 10 LSI profile for I²t short curves.

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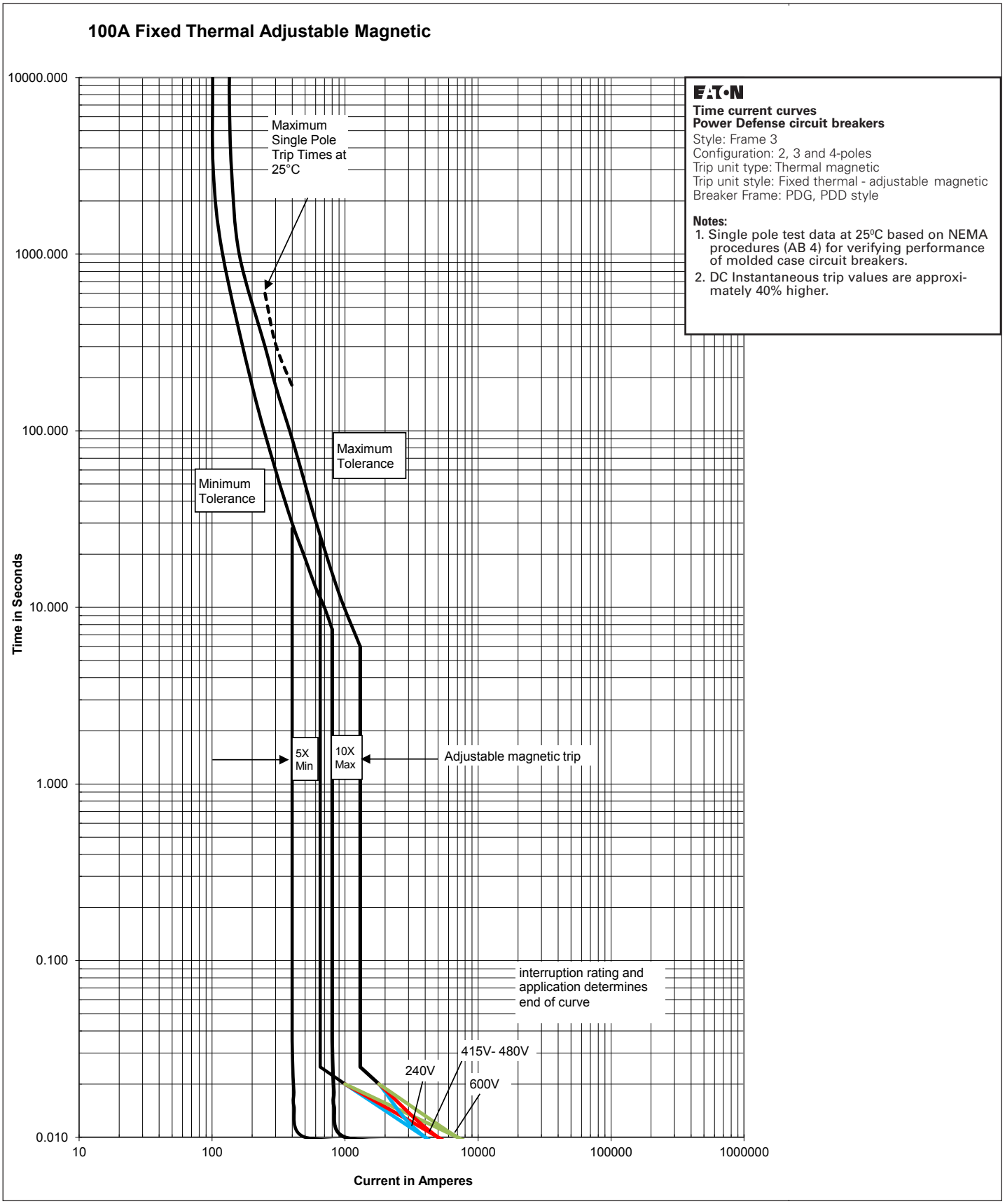

Figure 35. 100A fixed thermal adjustable magnetic.

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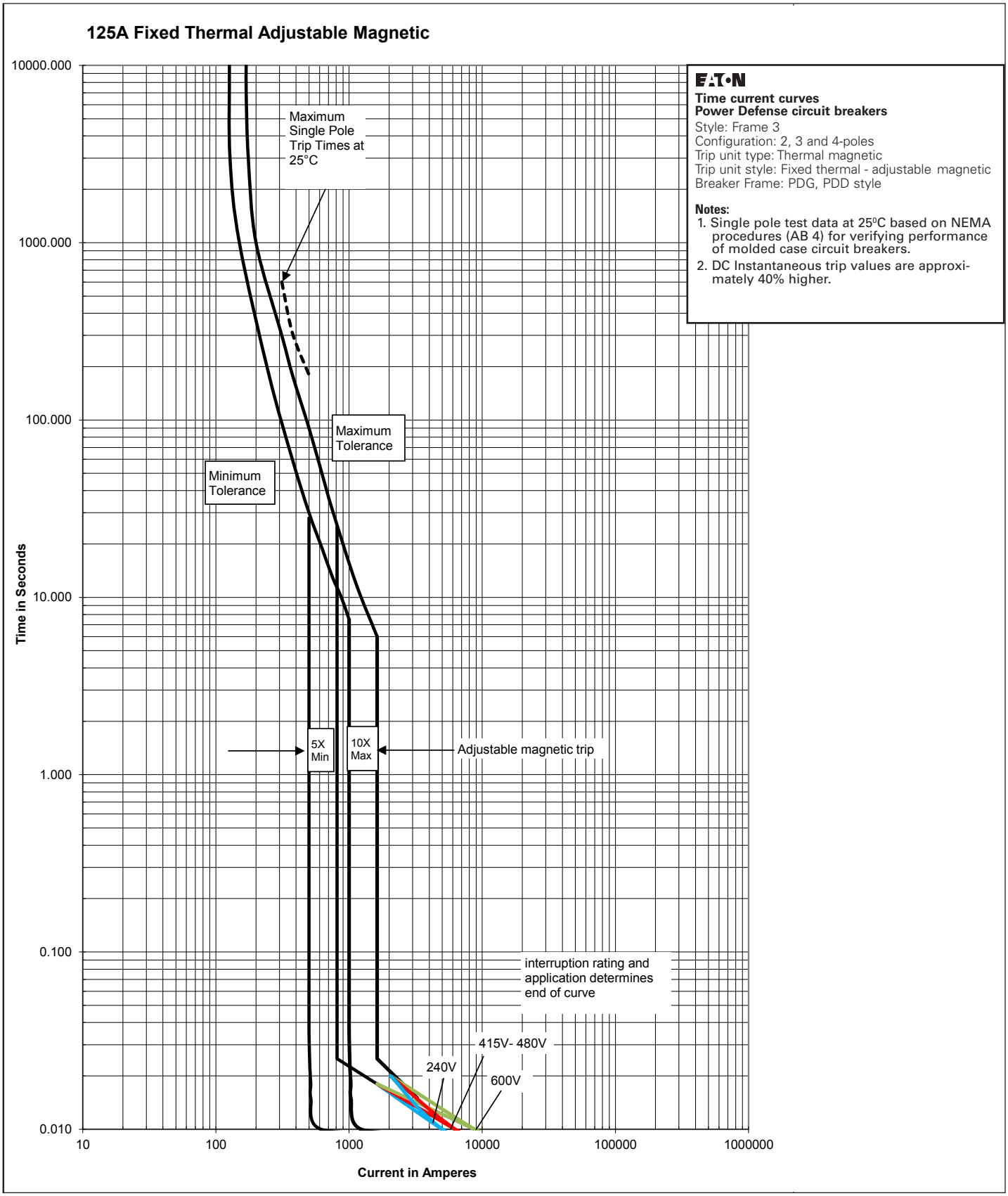

Figure 36. 125A fixed thermal adjustable magnetic.

January 2025

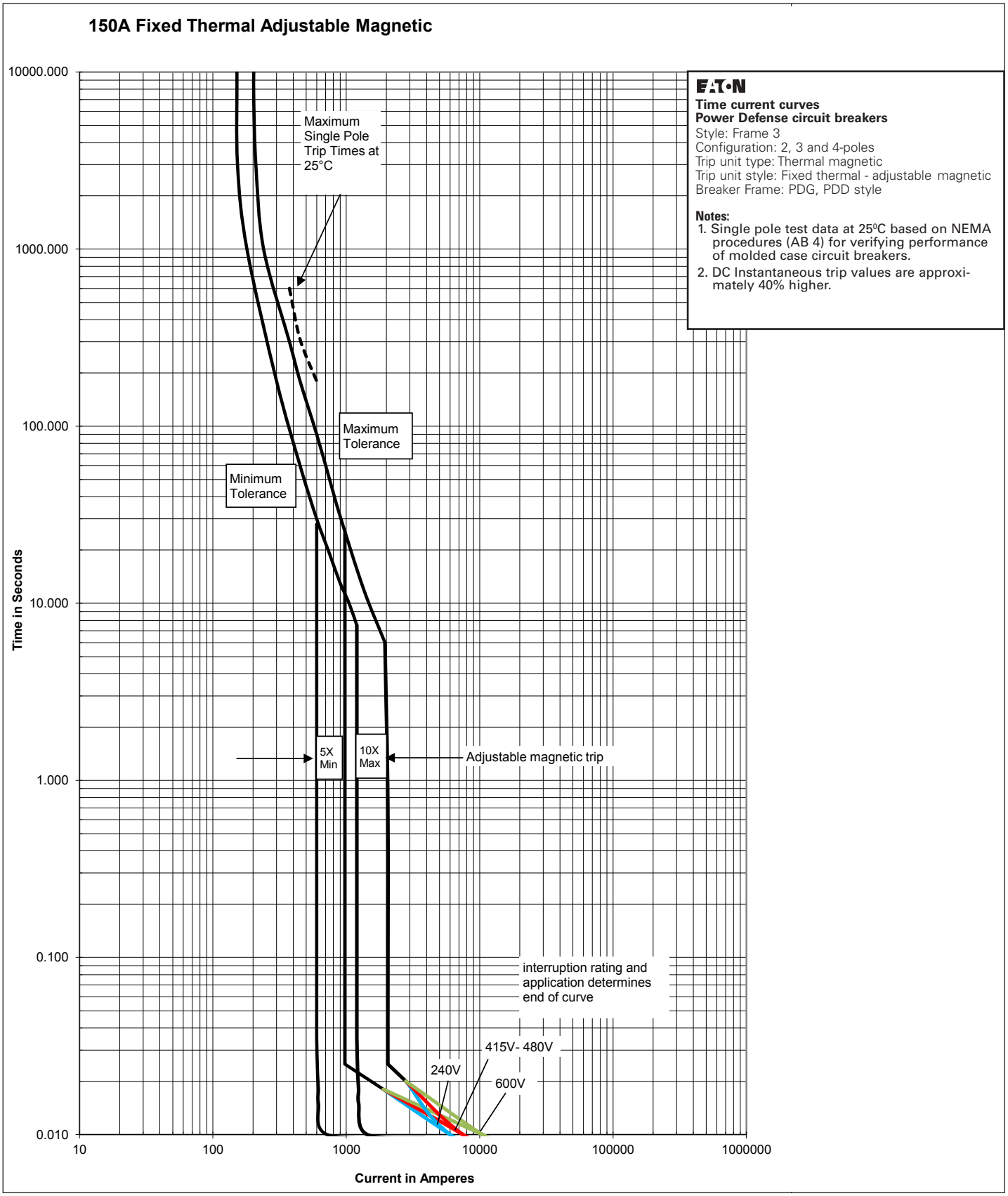

Figure 37. 150A fixed thermal adjustable magnetic.

January 2025

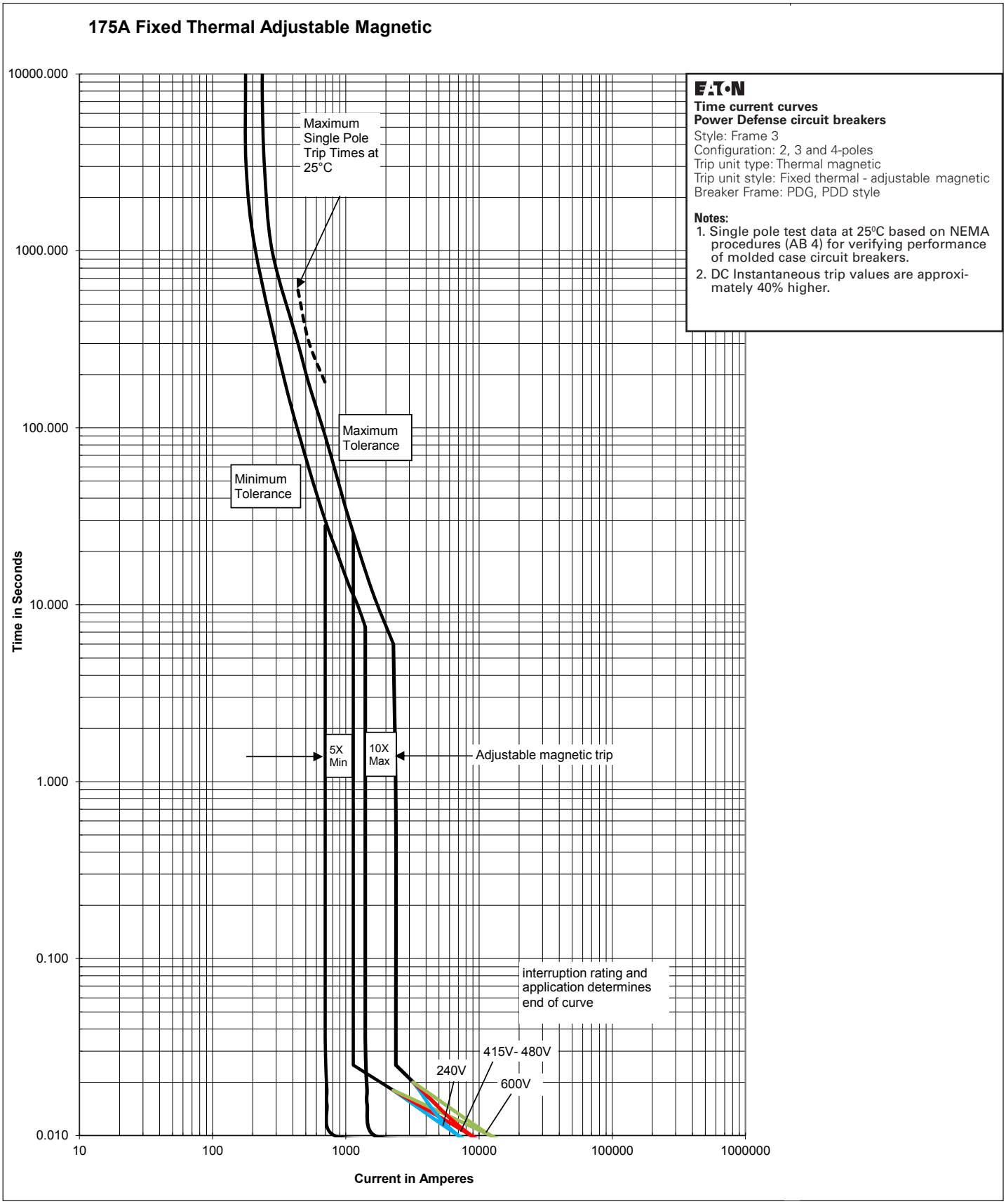

Figure 38. 175A fixed thermal adjustable magnetic.

January 2025

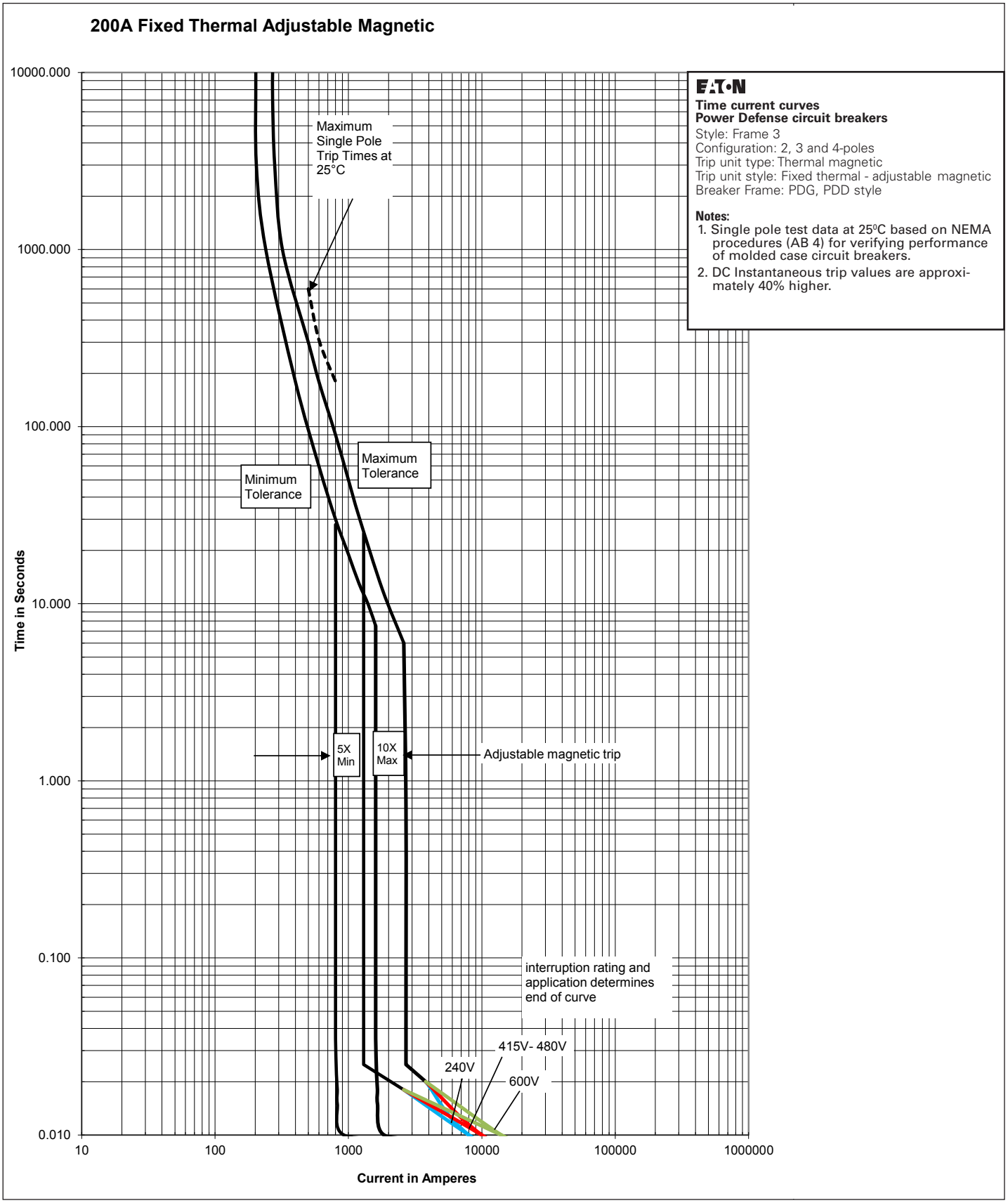

Figure 39. 200A fixed thermal adjustable magnetic.

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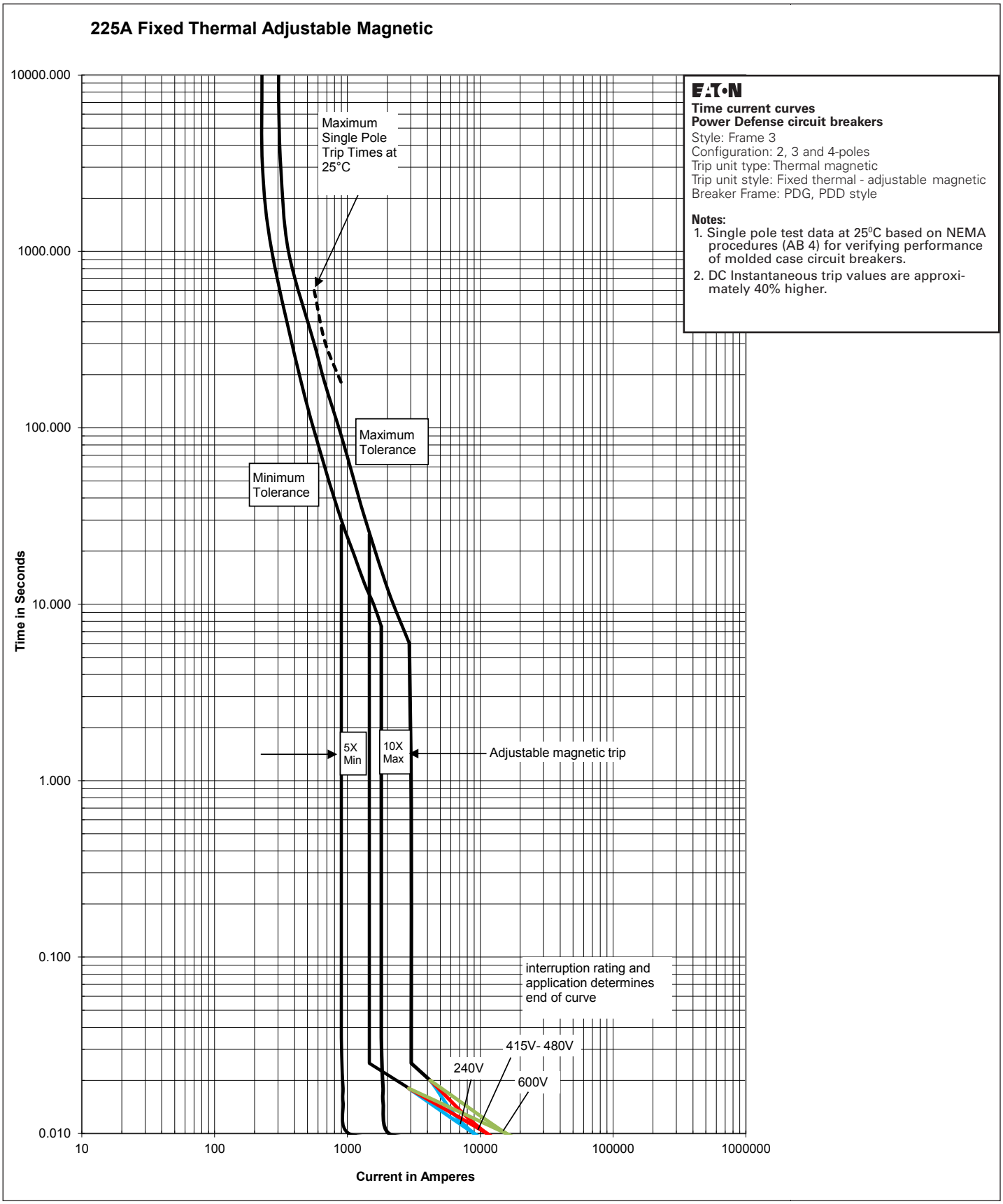

Figure 40. 225A fixed thermal adjustable magnetic.

January 2025

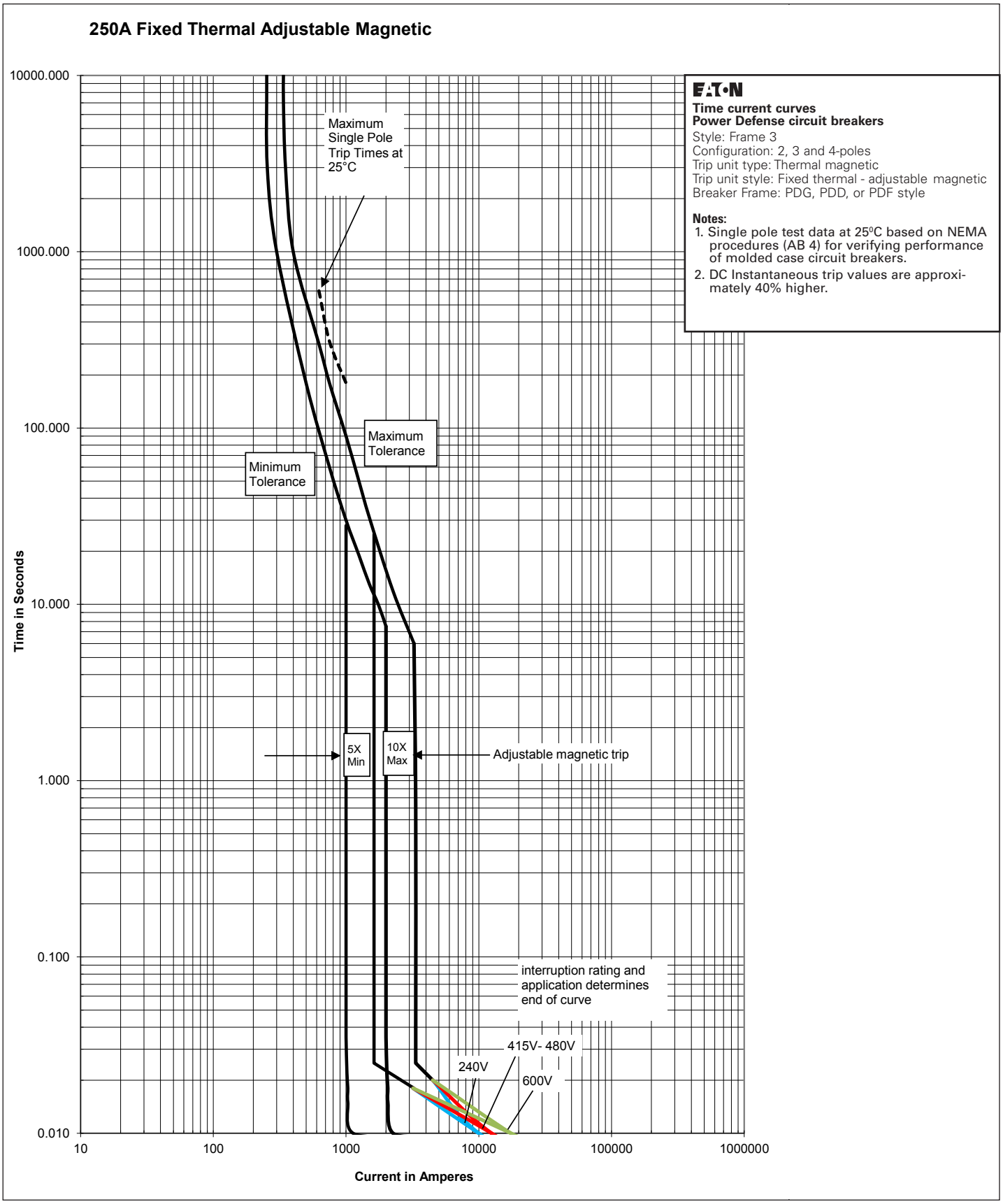

Figure 41. 250A fixed thermal adjustable magnetic.

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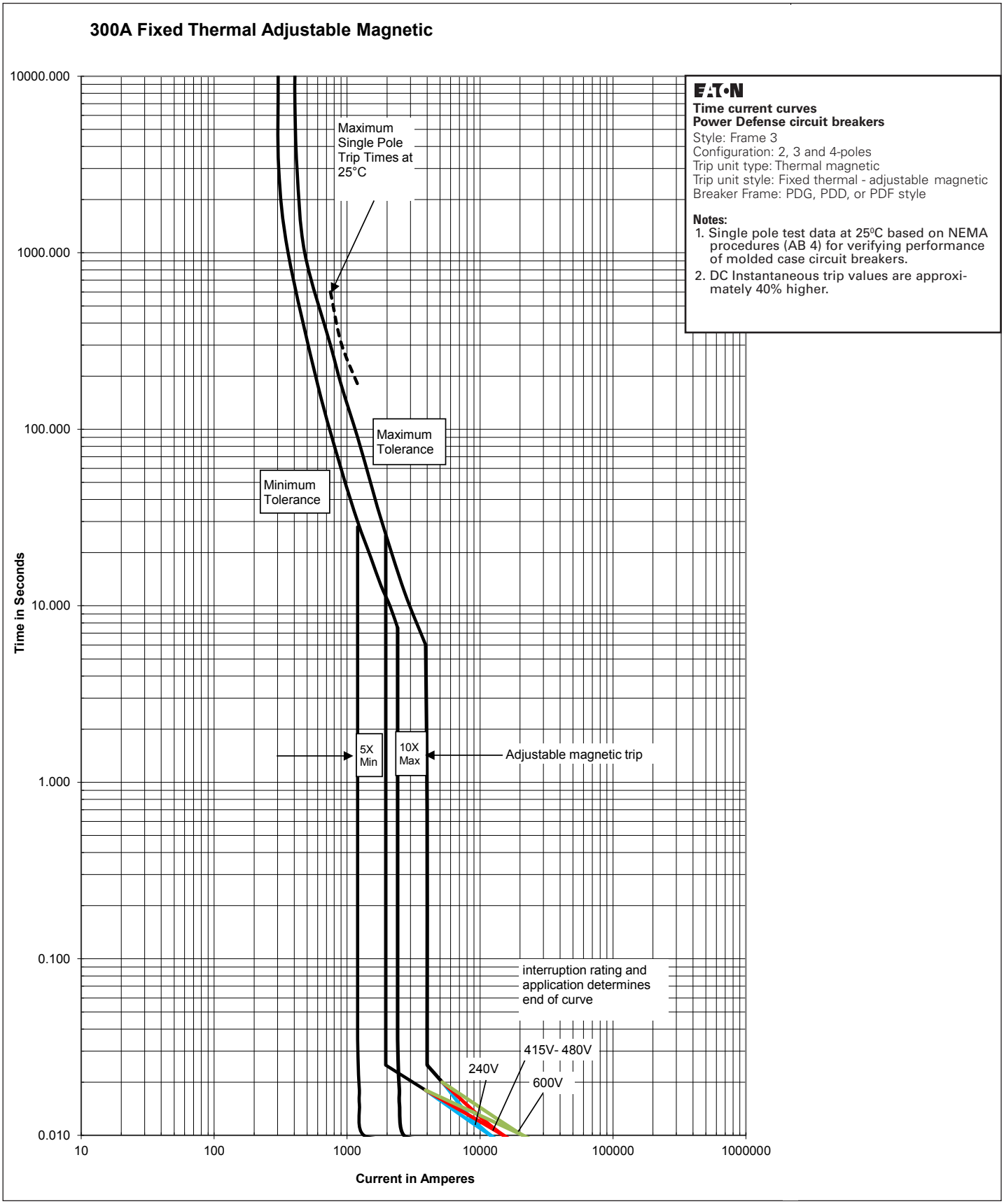

Figure 42. 300A fixed thermal adjustable magnetic.

January 2025

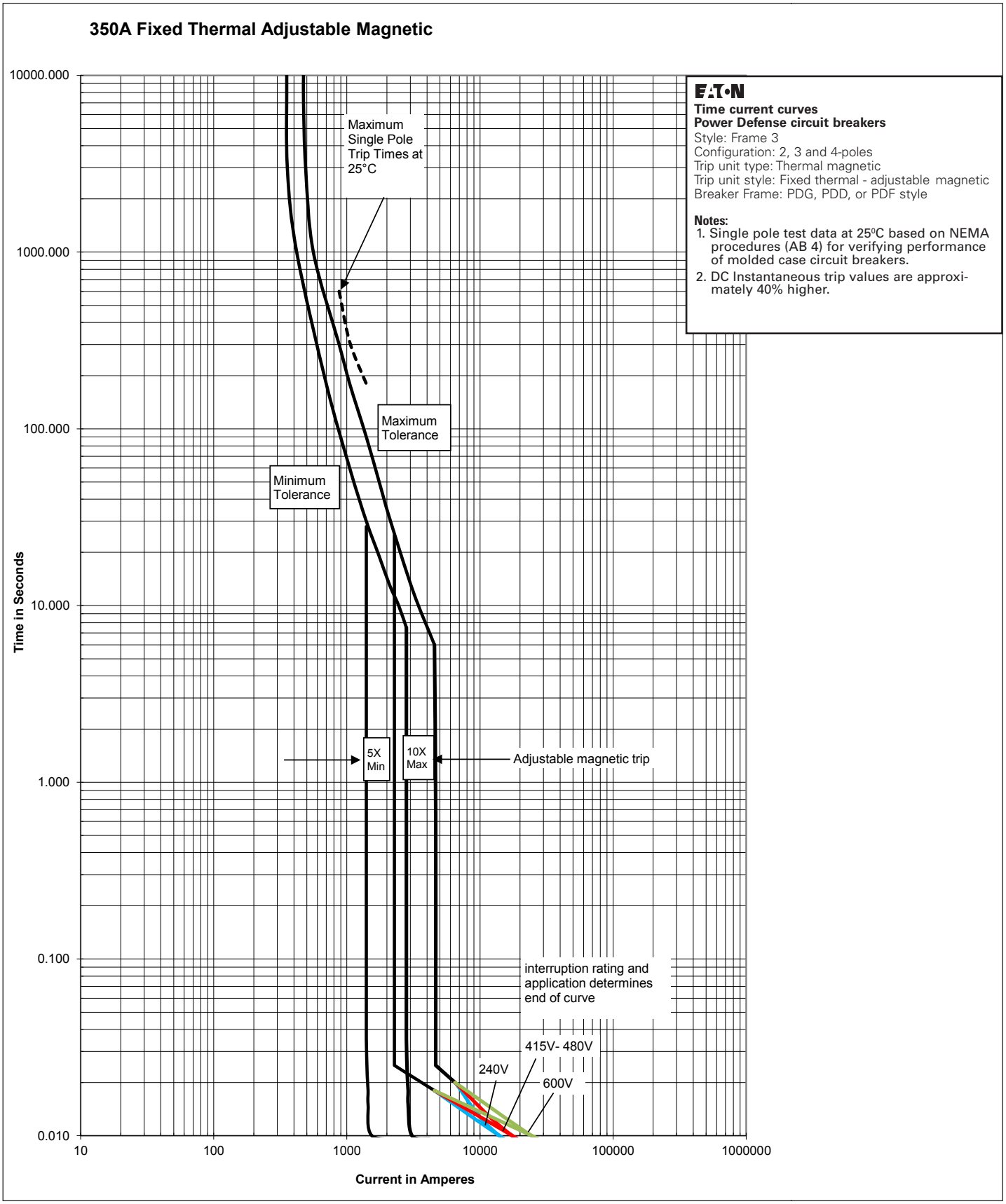

Figure 43. 350A fixed thermal adjustable magnetic.

January 2025

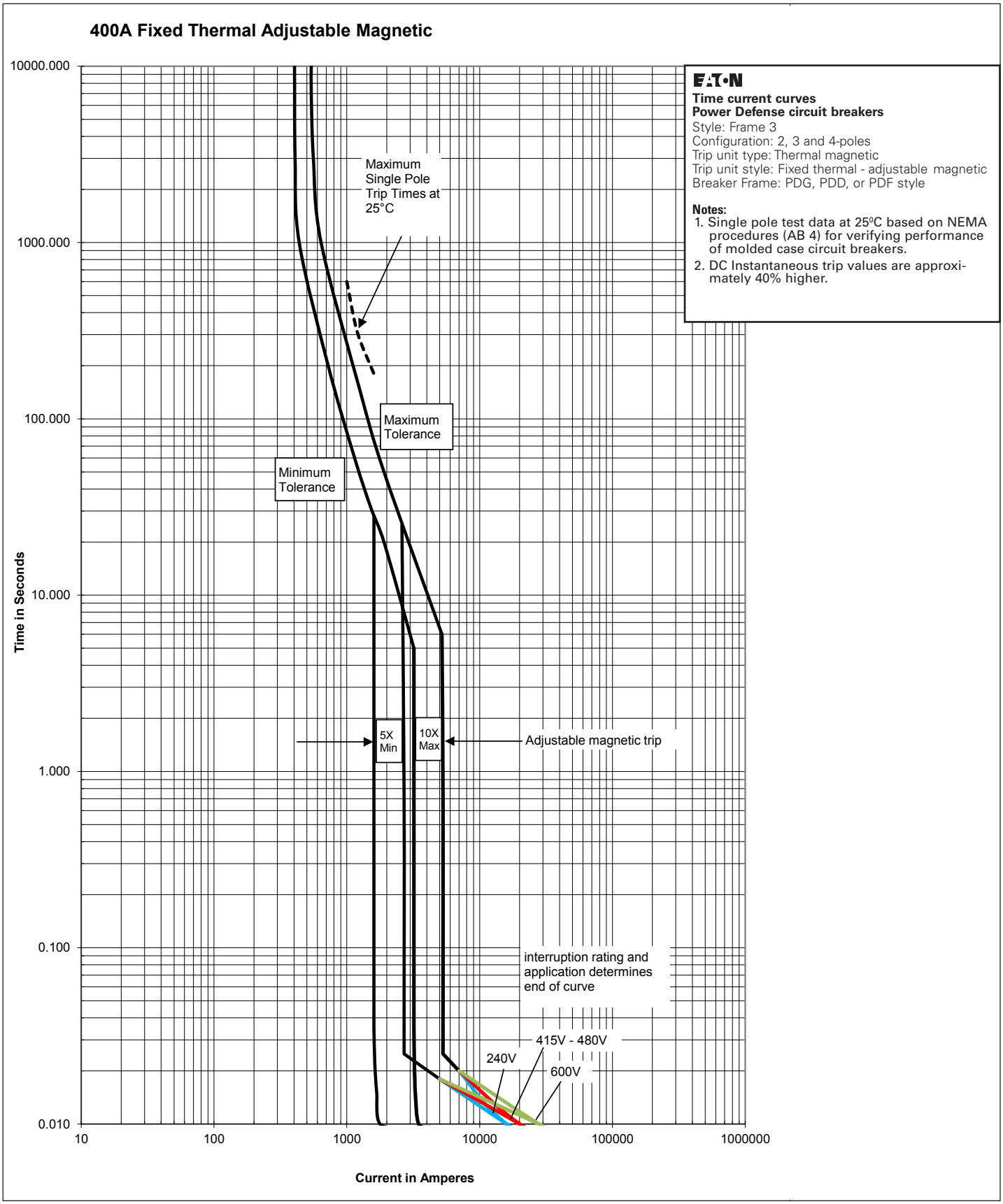

Figure 44. 400A fixed thermal adjustable magnetic.

January 2025

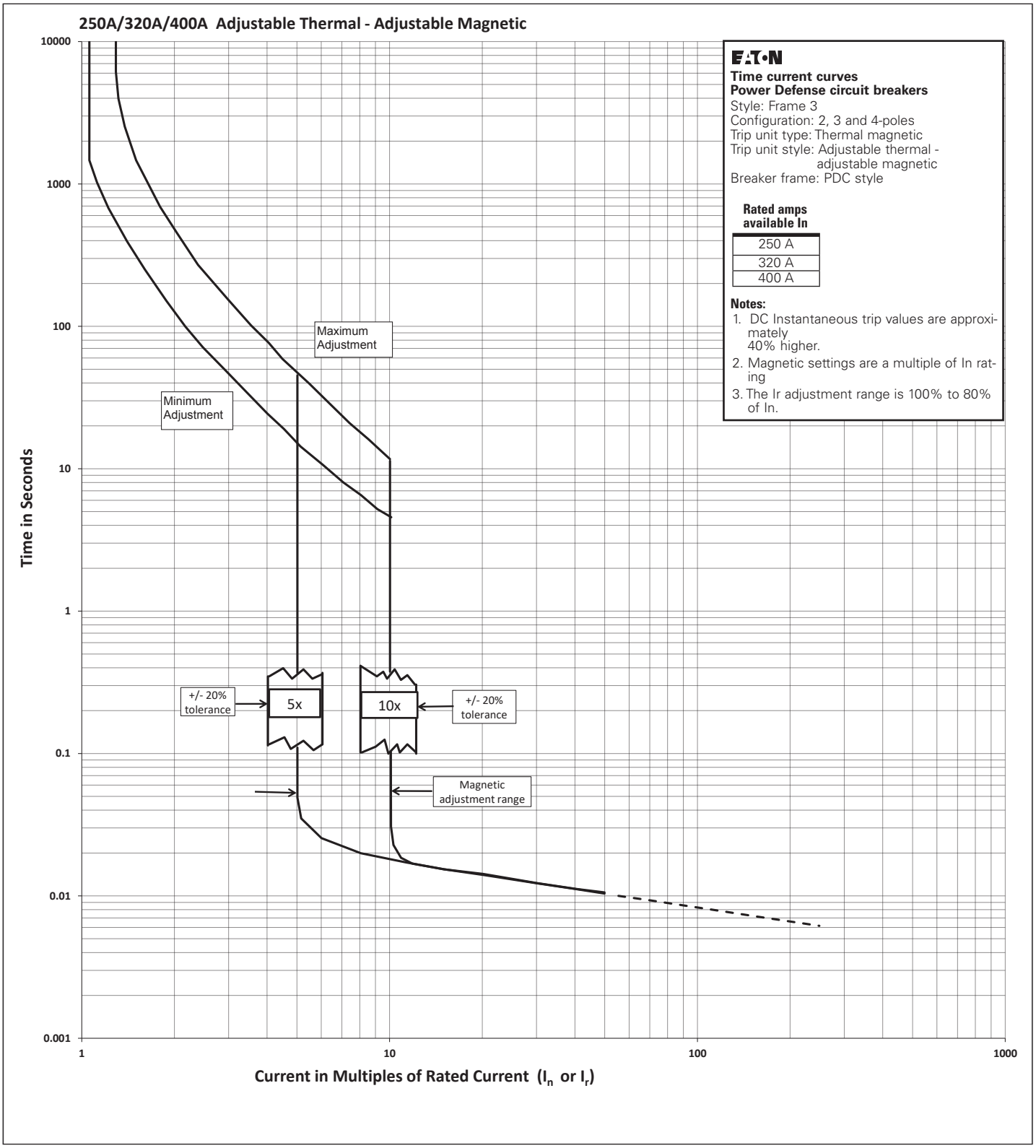

Figure 45. 250A/320A/400A adjustable thermal adjustable magnetic.

January 2025

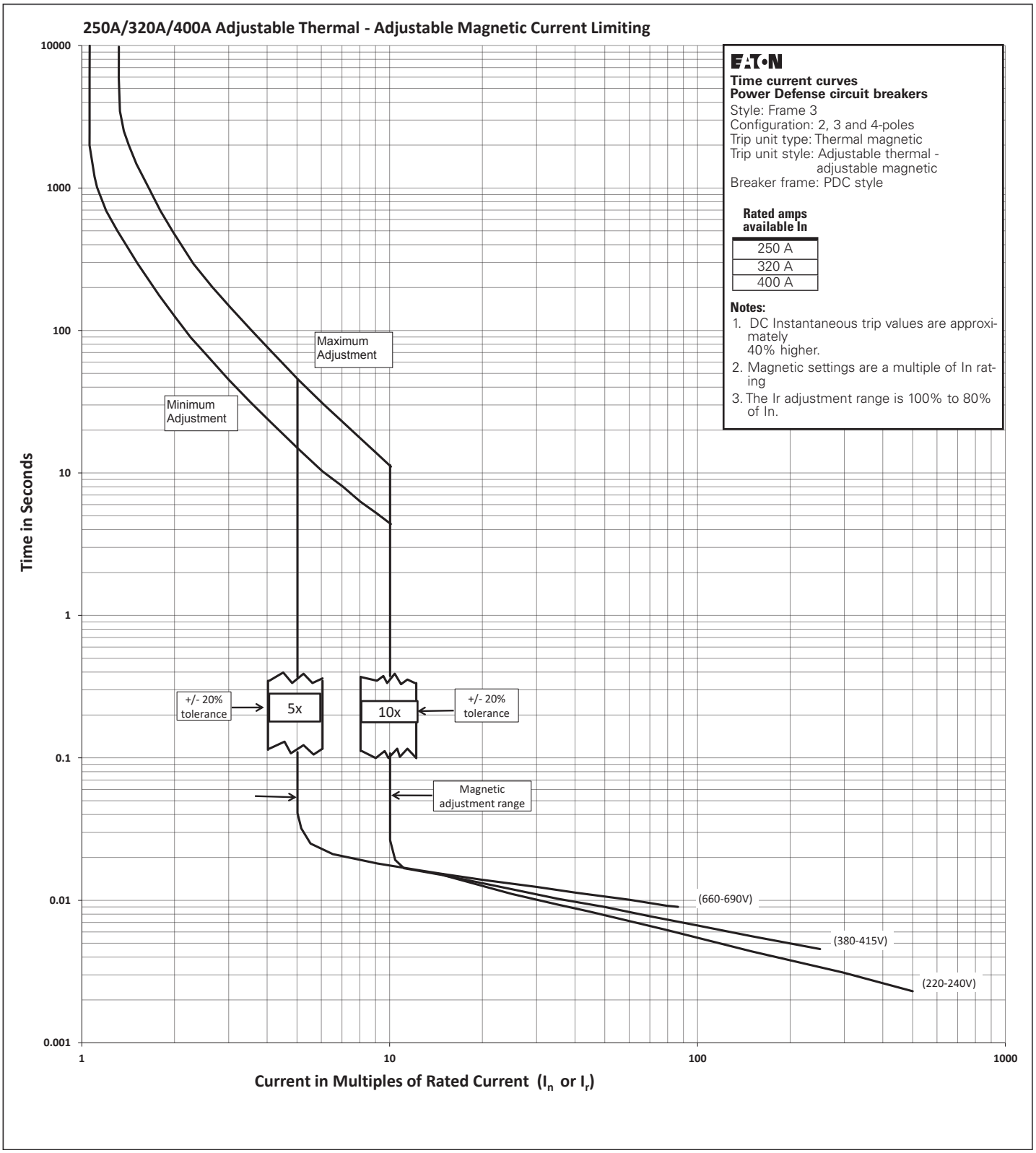

Figure 46. 250A/320A/400A adjustable thermal adjustable magnetic - current limiting. **January 2025**

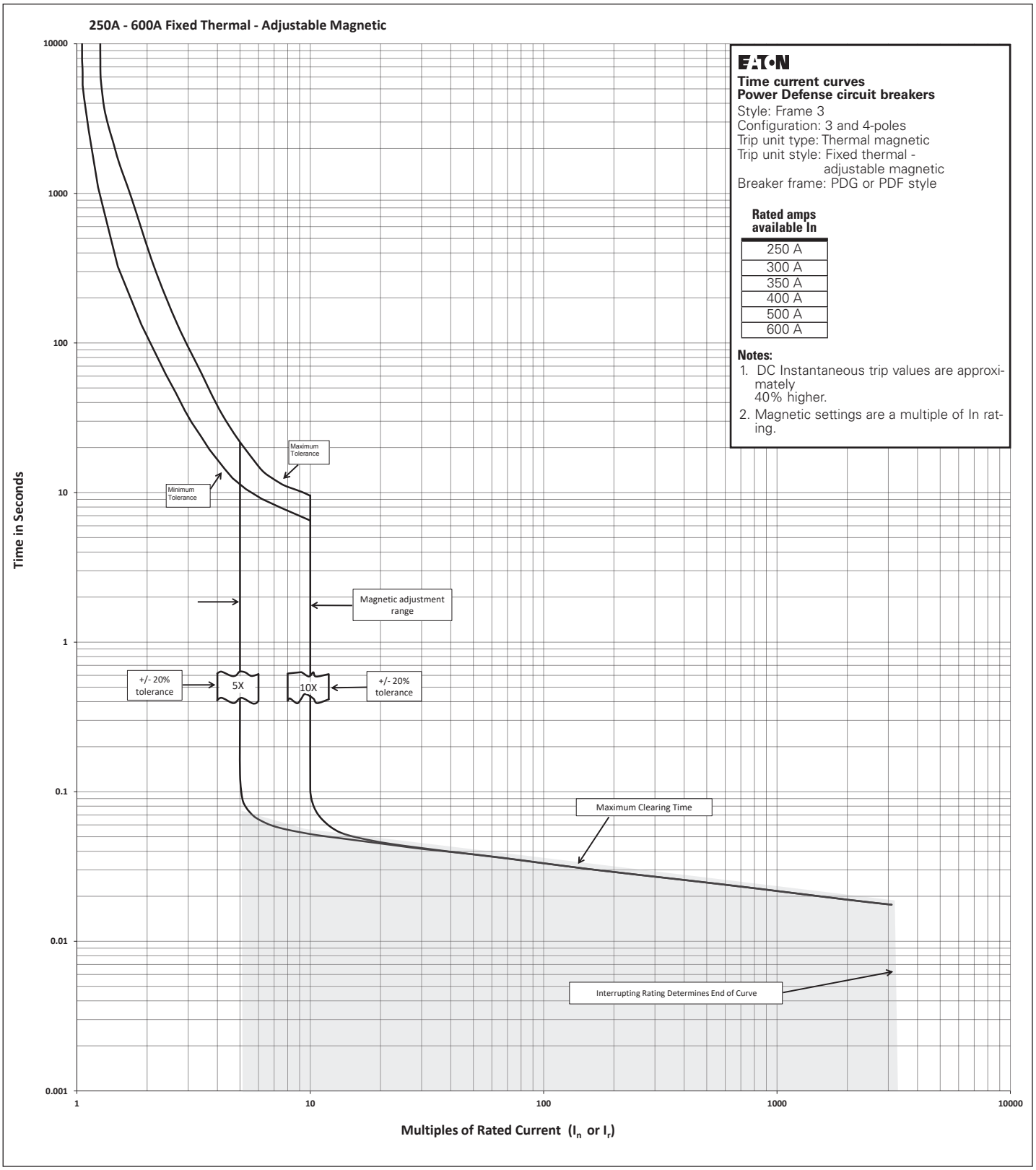

Figure 47. 250A – 600A fixed thermal adjustable magnetic.

January 2025

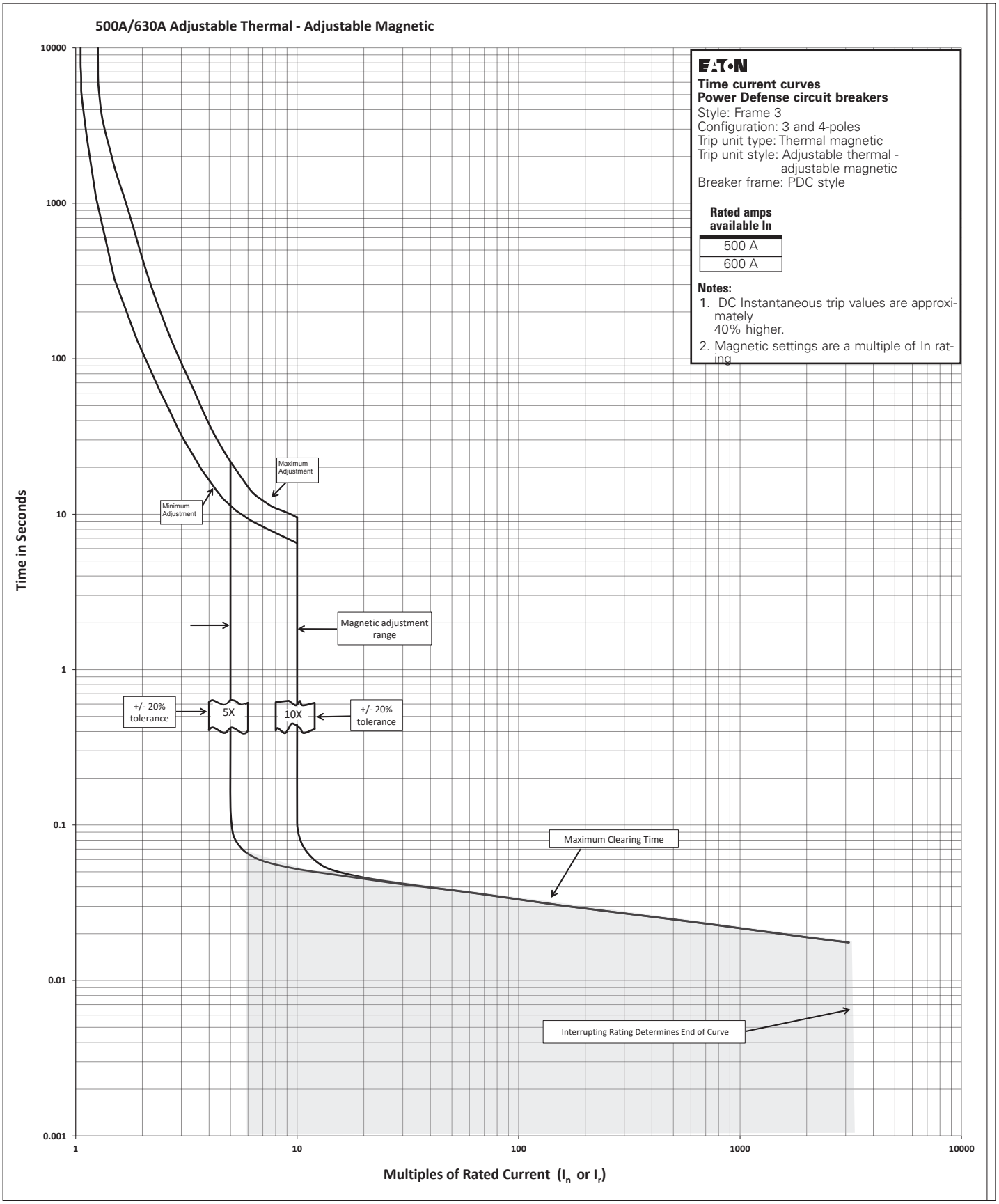

Figure 48. 500A/630A adjustable thermal adjustable magnetic.

January 2025

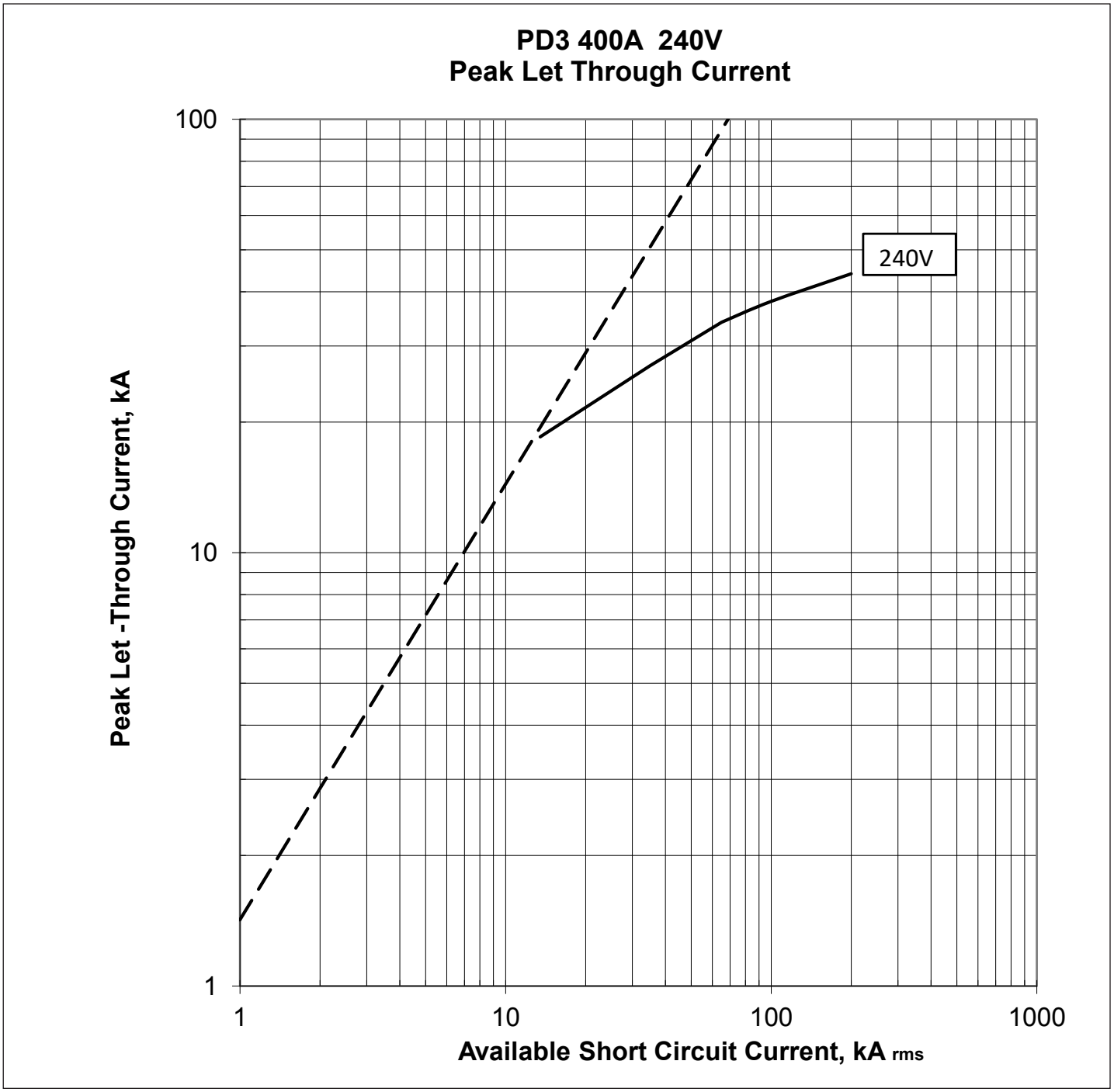

Figure 49. Peak let through current 400A @ 240V.

January 2025

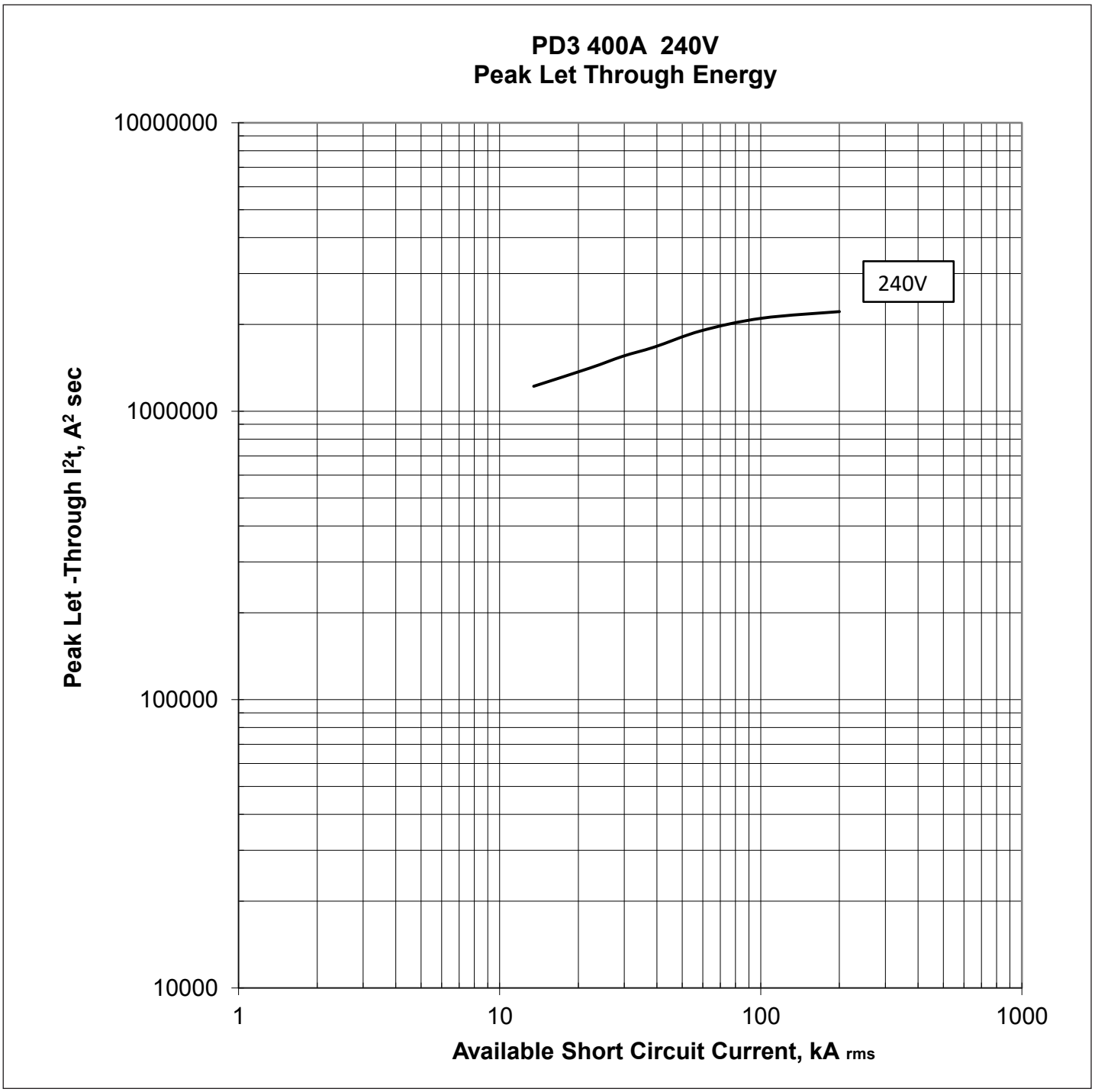

Figure 50. Peak let through energy 400A @ 240V.

January 2025

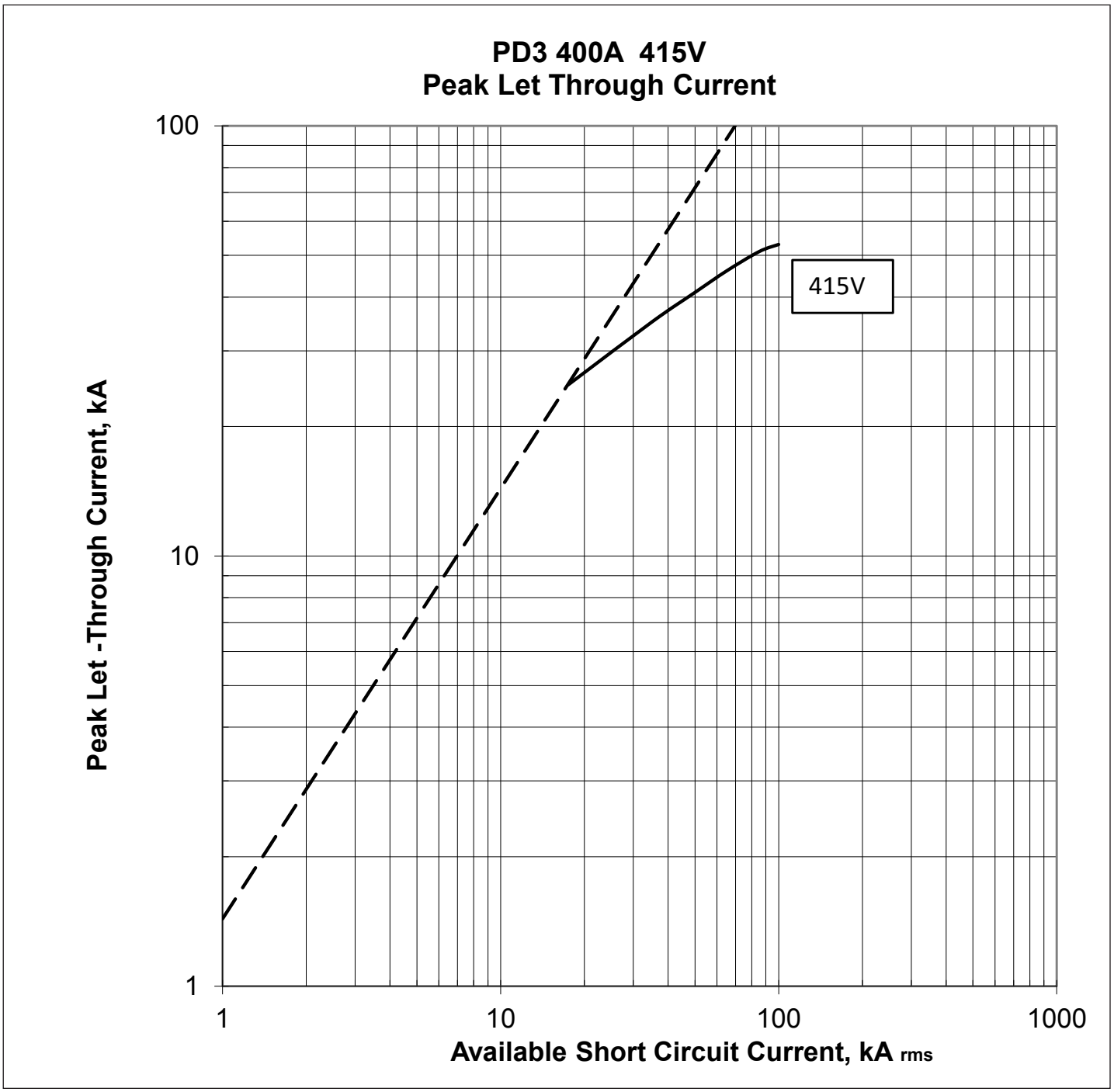

Figure 51. Peak let through current 400A @ 415V.

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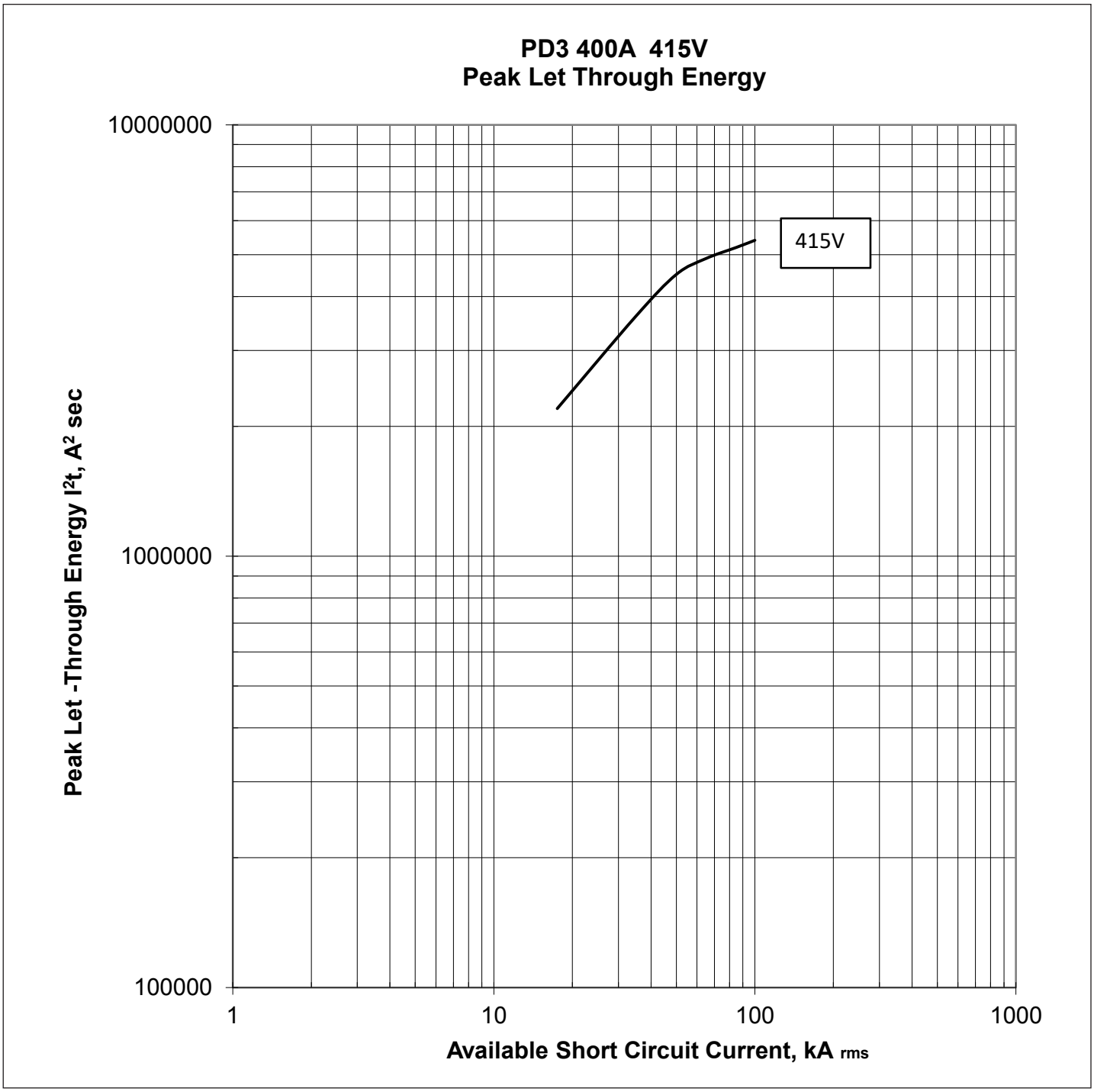

Figure 52. Peak let through energy 400A @ 415V.

January 2025

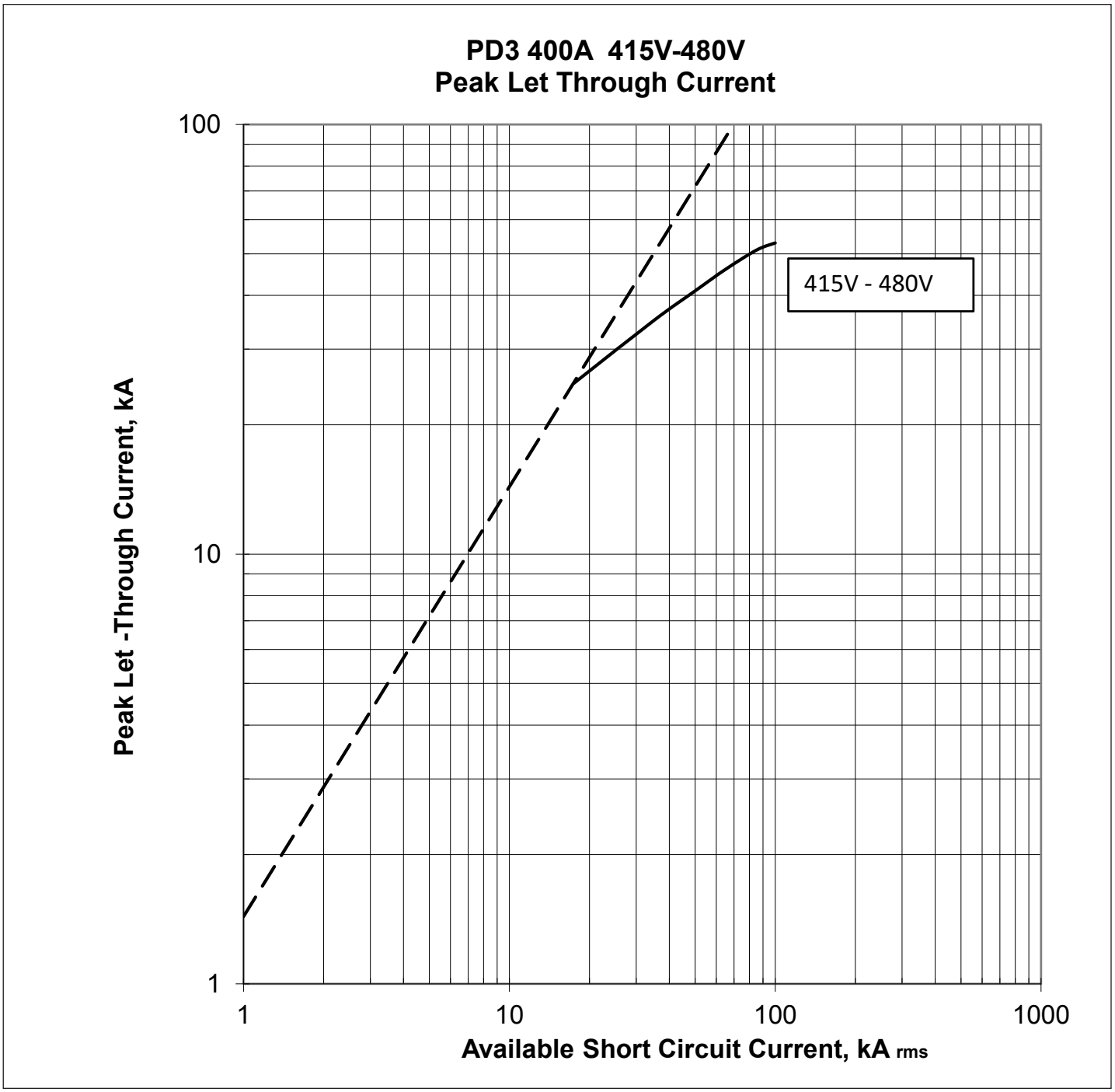

Figure 53. Peak let through current 400A @ 415V-480V.

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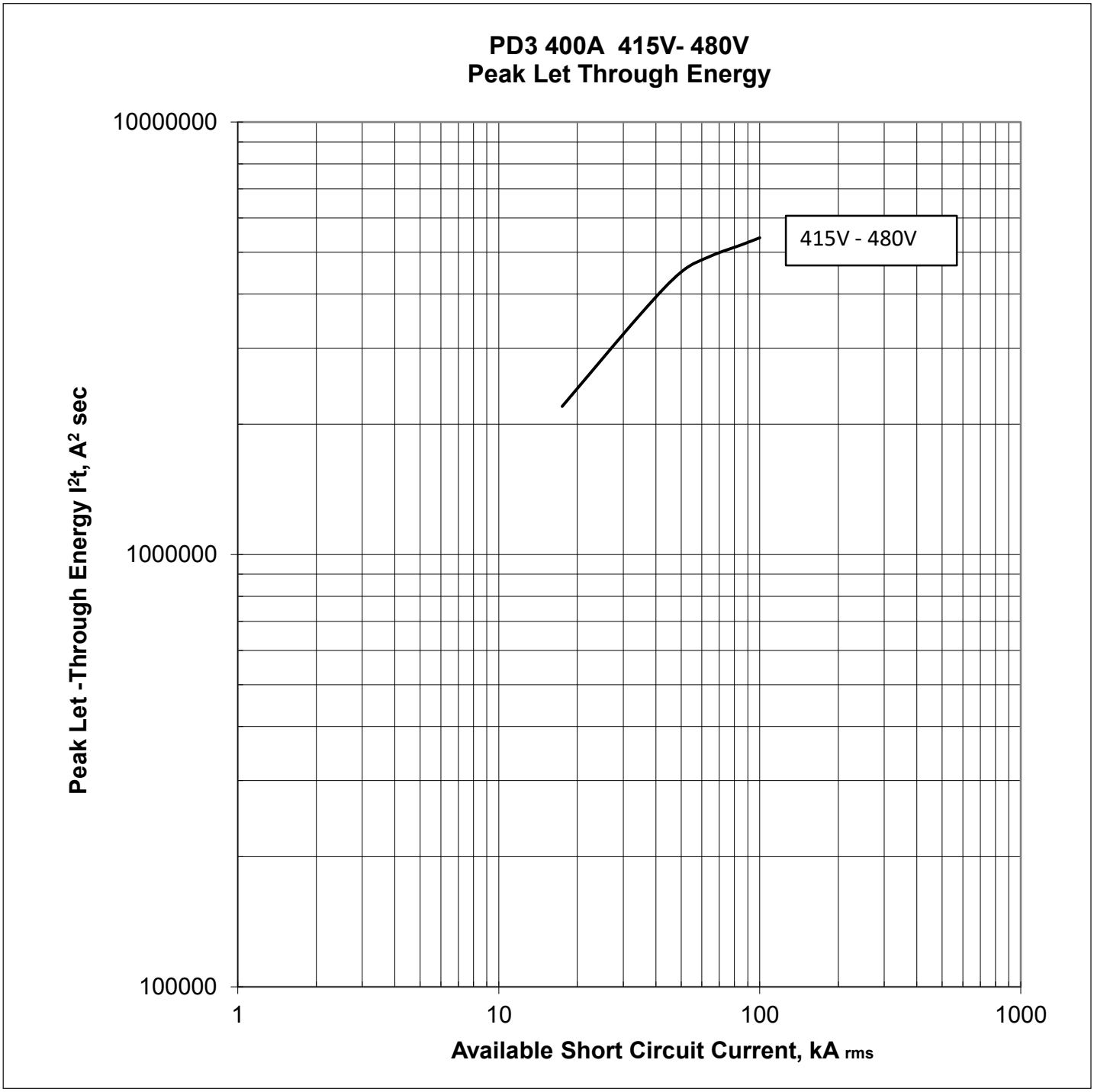

Figure 54. Peak let through energy 400A @ 415V-480V.

January 2025

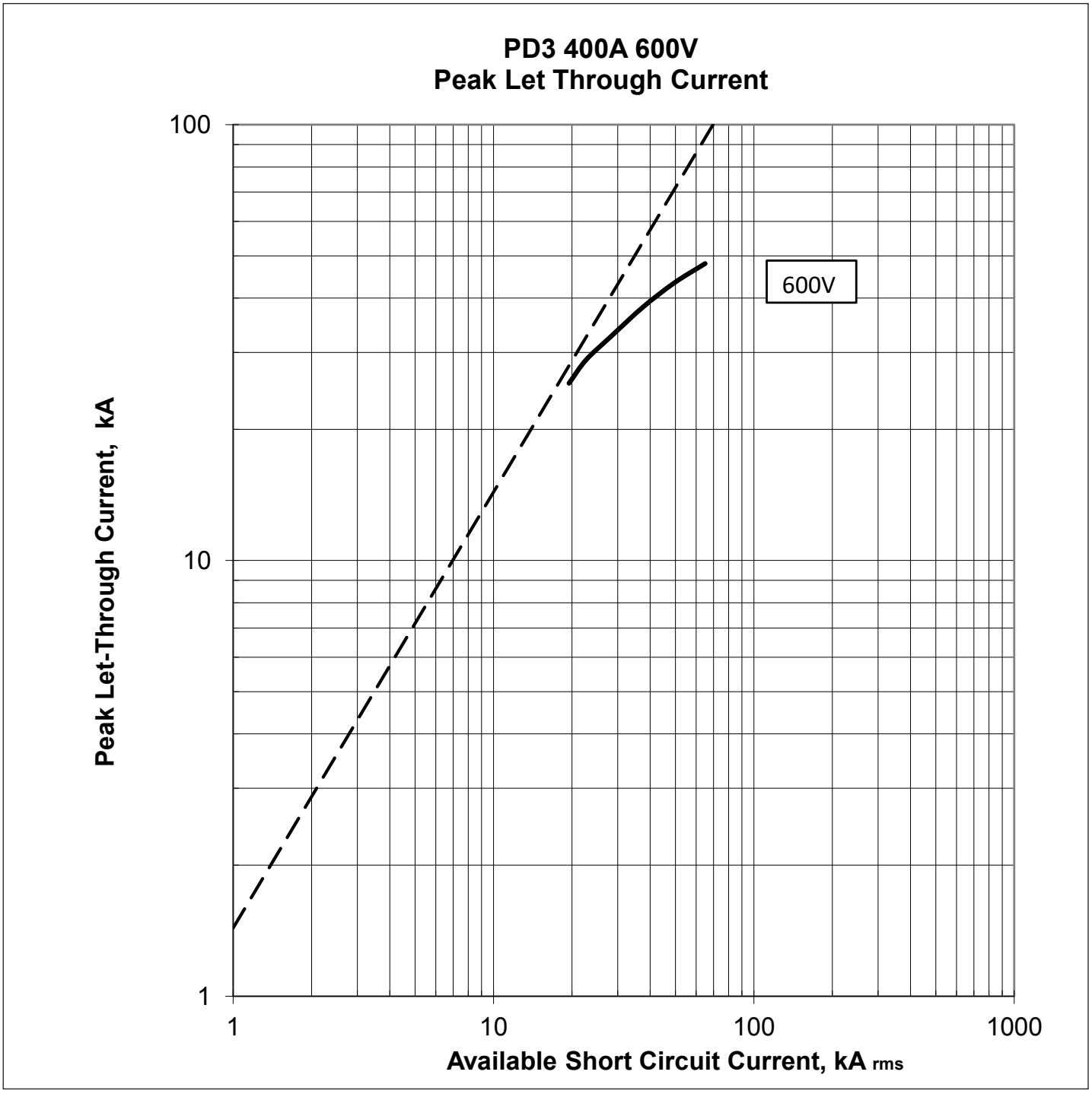

Figure 55. Peak let through current 400A @ 600V.

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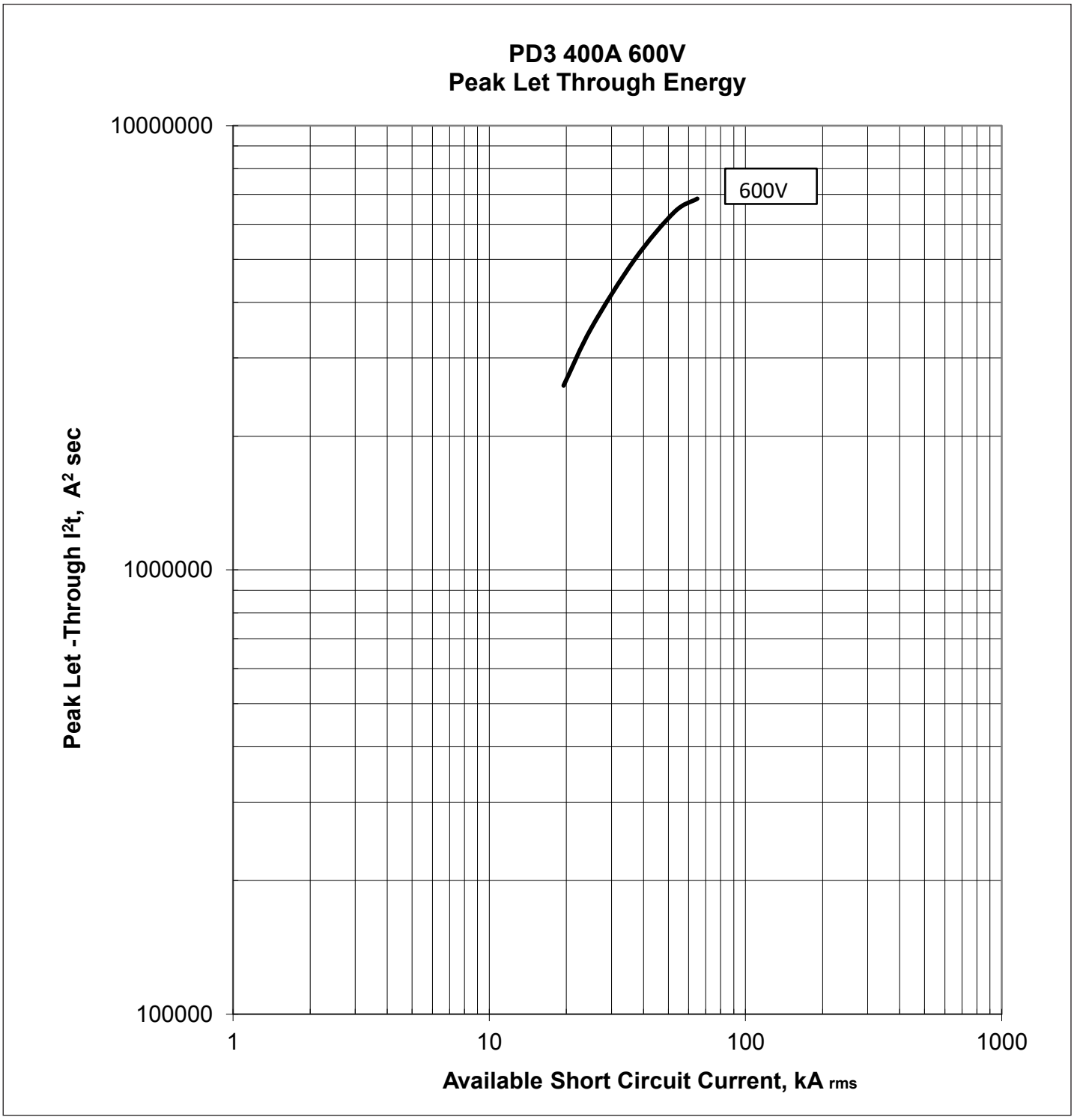

Figure 56. Peak let through energy 400A @ 600V

January 2025

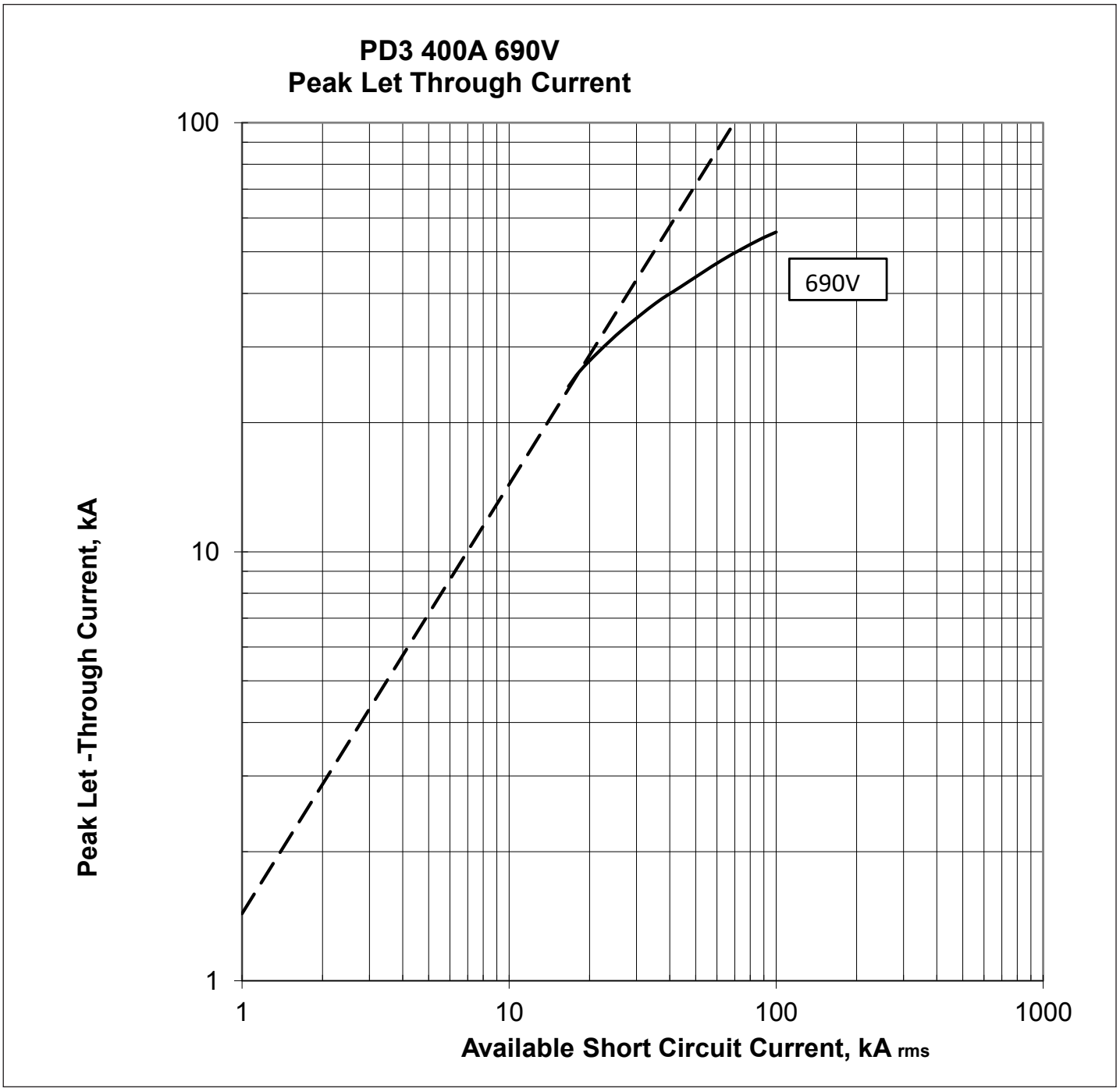

Figure 57. Peak let through current 400A @ 690V.

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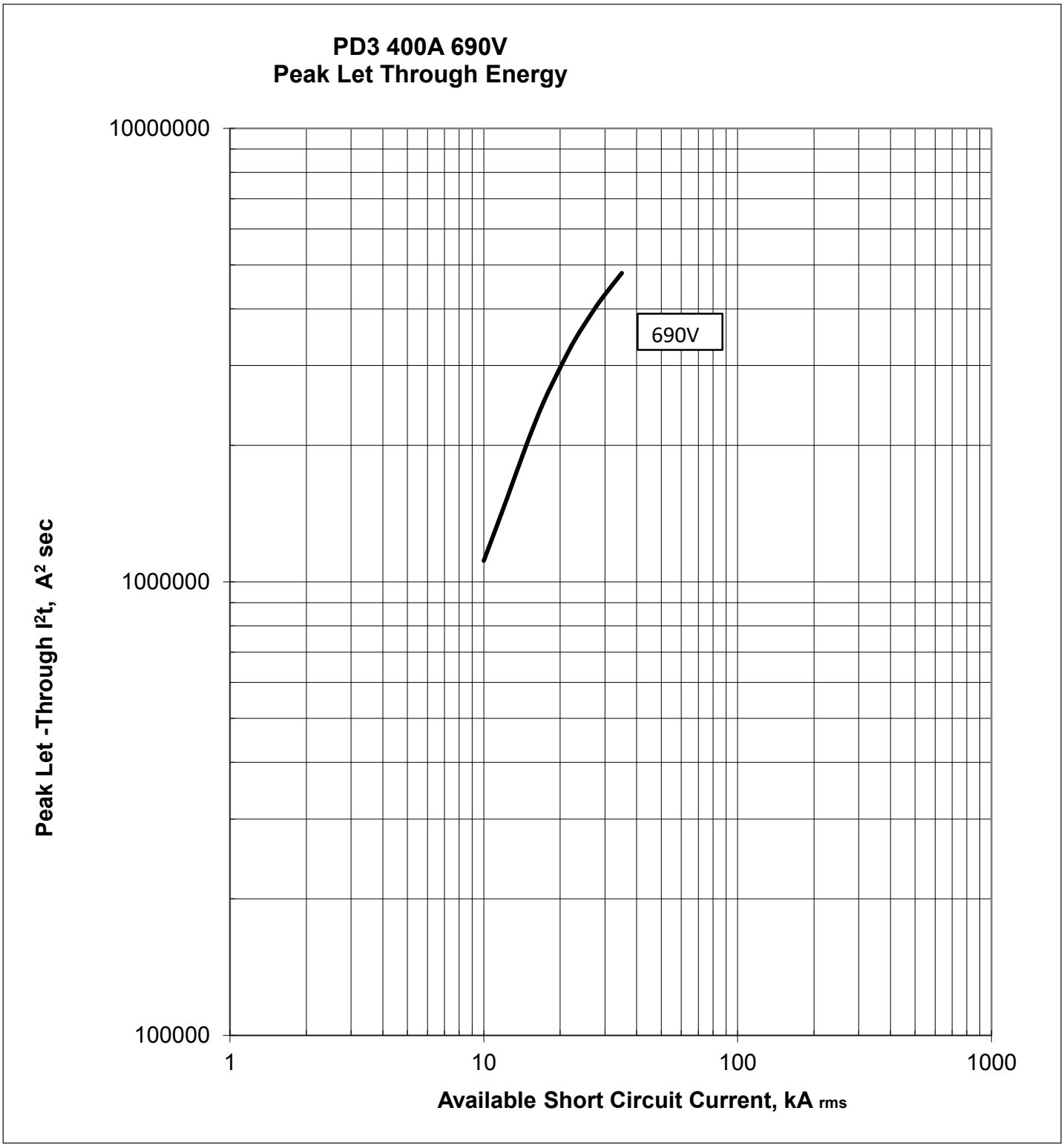

Figure 58. Peak let through energy 400A @ 690V.

January 2025

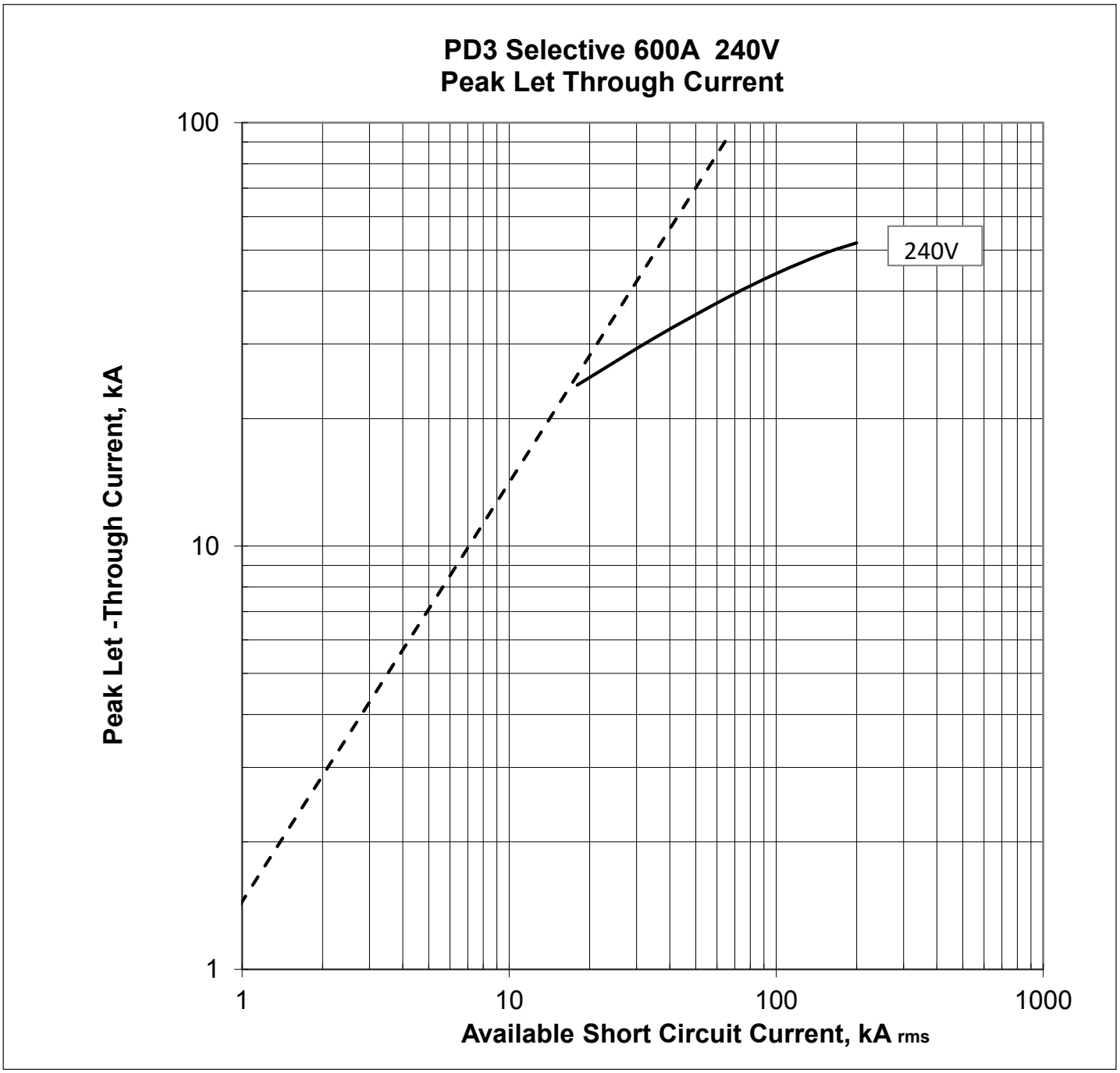

Figure 59. Peak let through current selective frames 600A @ 240V.

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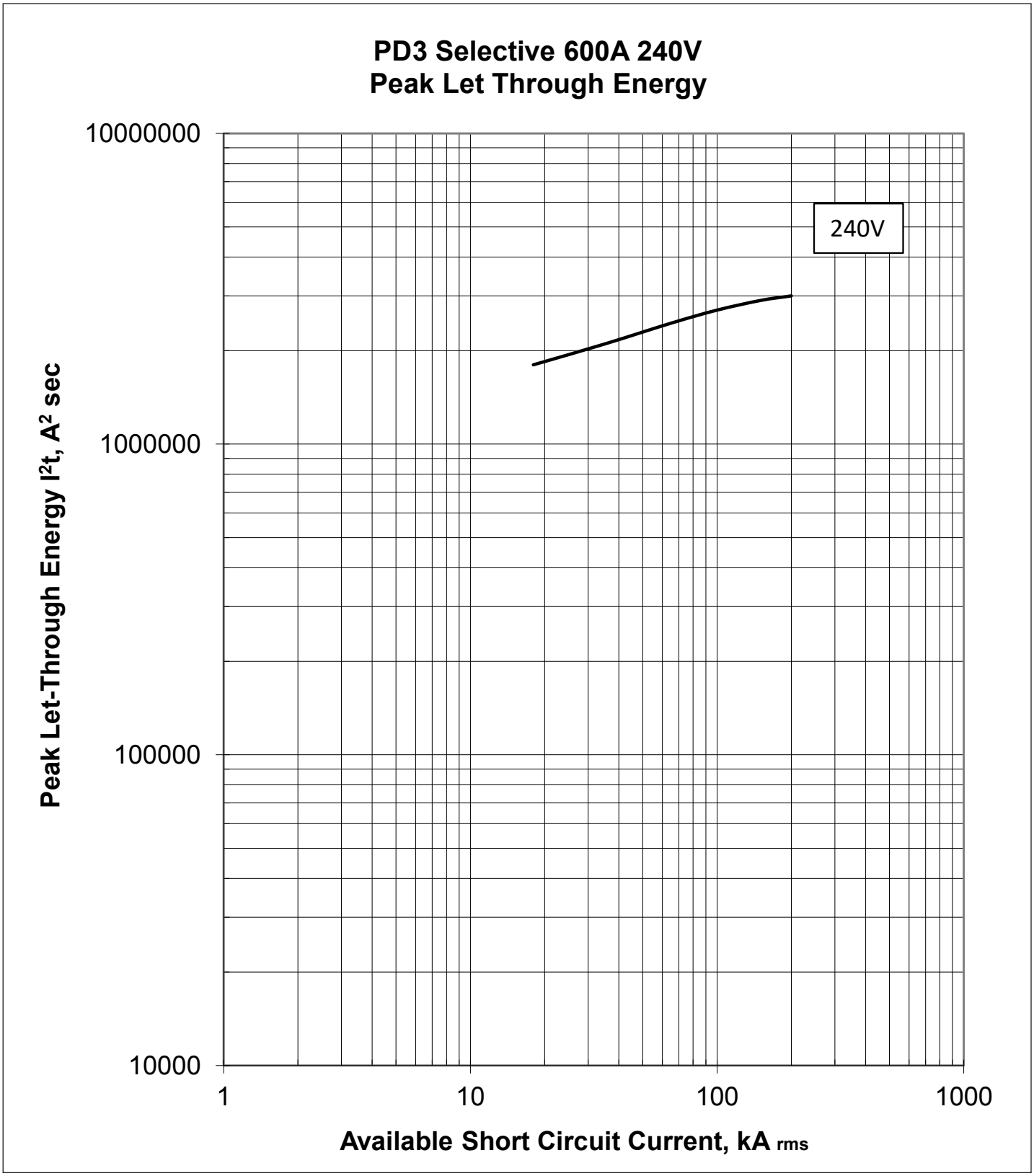

Figure 60. Peak let through energy selective frames 600A @ 240V.

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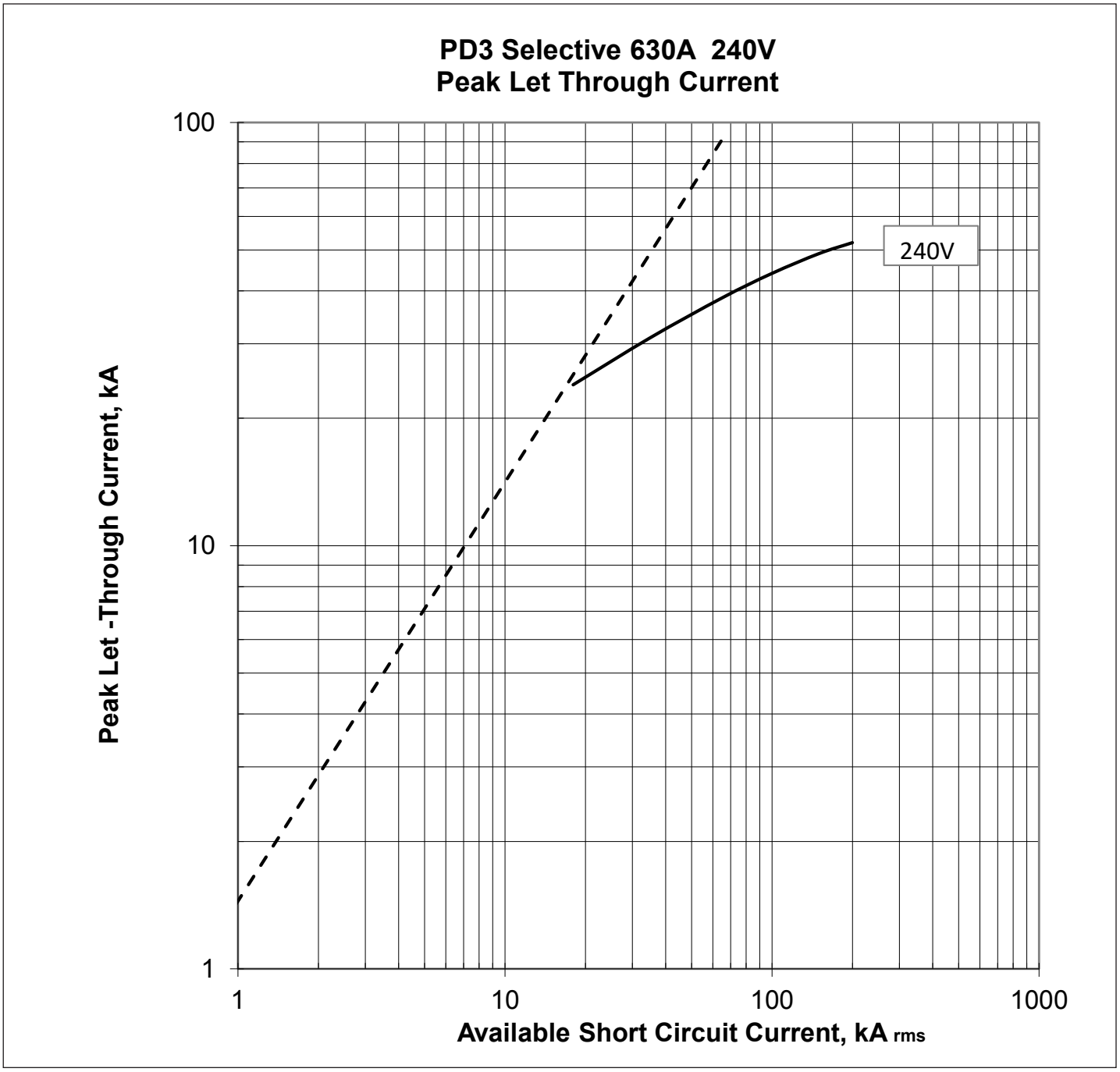

Figure 61. Peak let through current selective frames 630A @ 240V.

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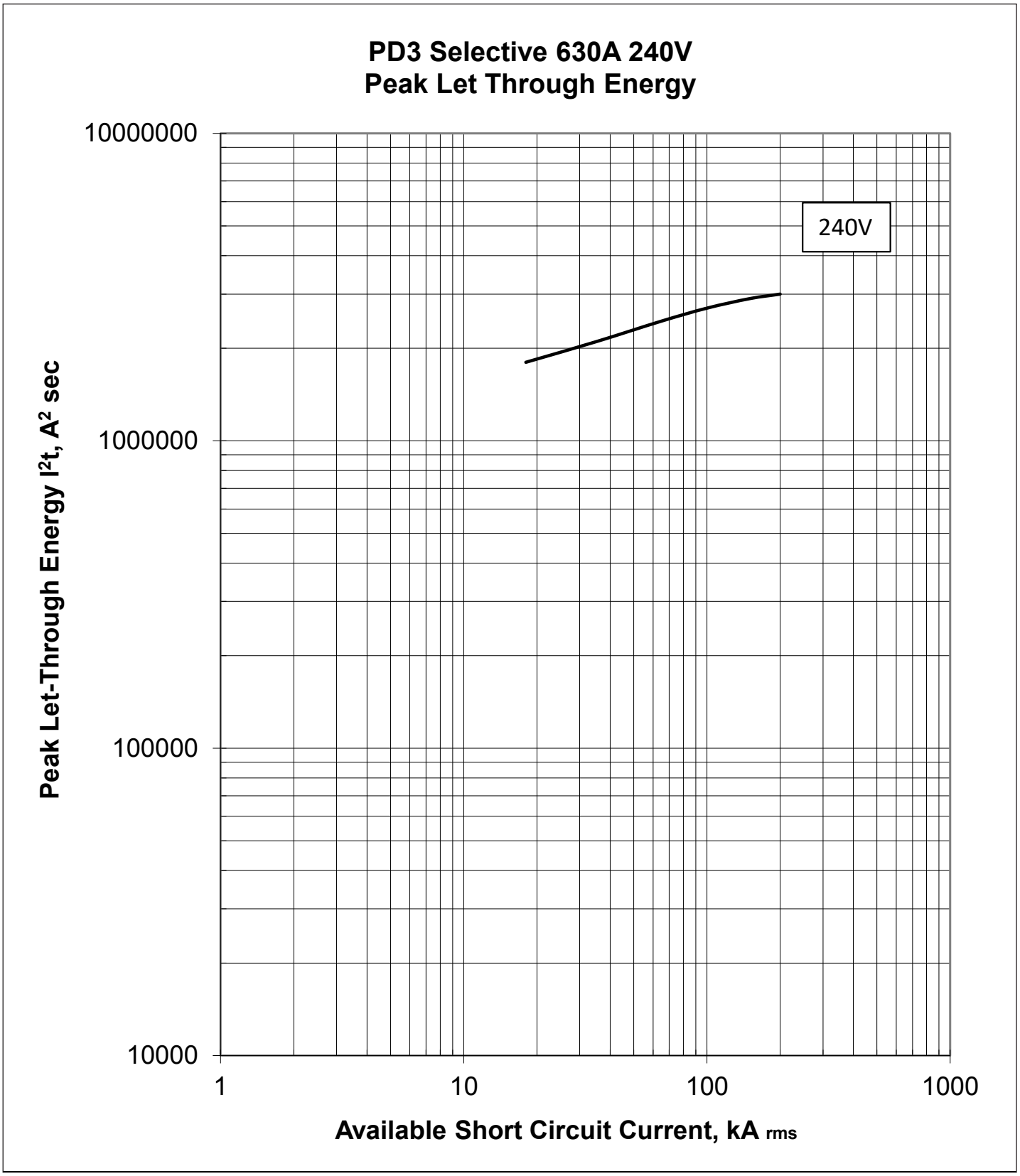

Figure 62. Peak let through energy selective frames 630A @ 240V. **January 2025.**

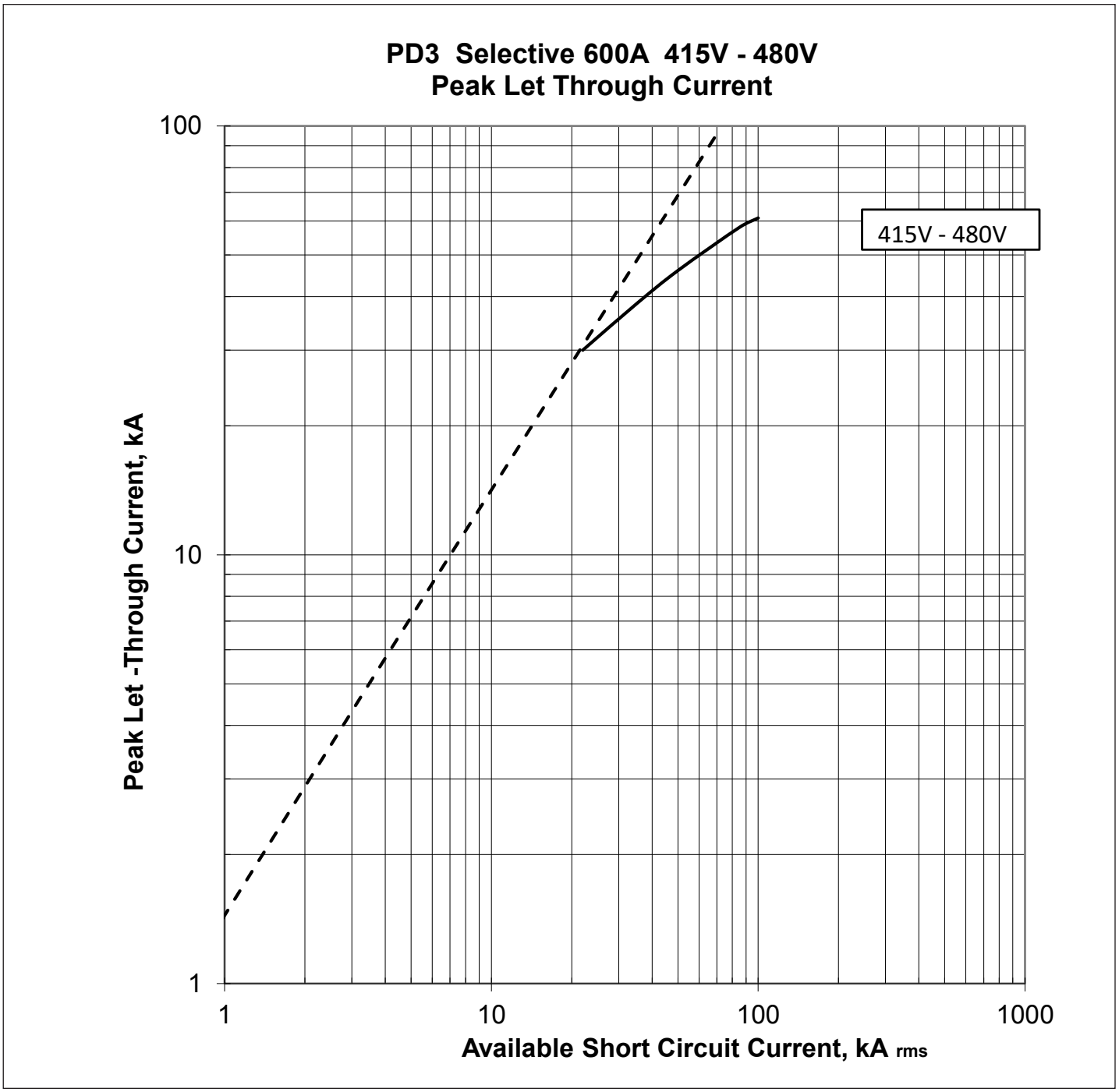

Figure 63. Peak let through current selective 600A @ 415V-480V.

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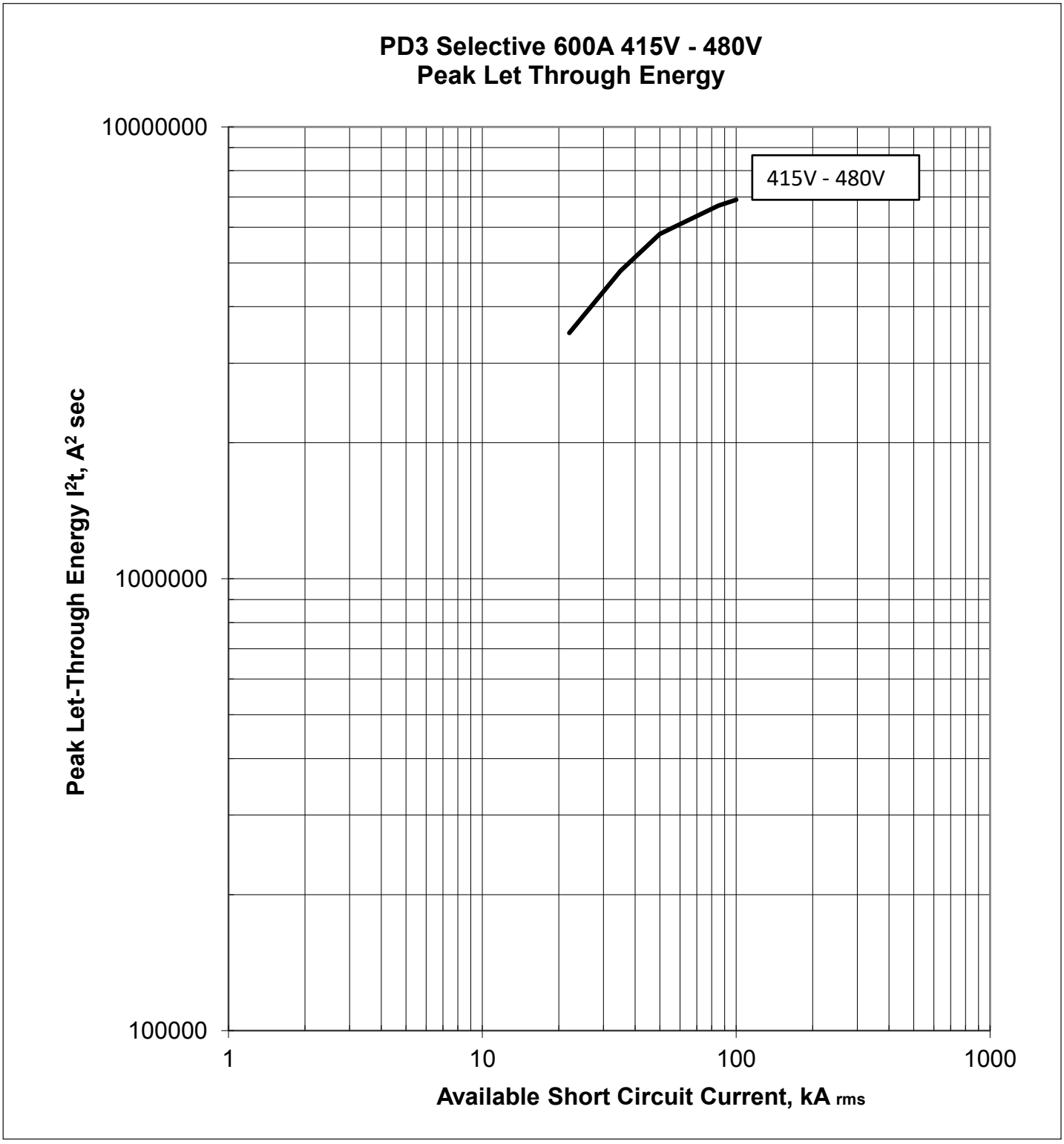

Figure 64. Peak let through energy selective 600A @ 415V-480V.

January 2025

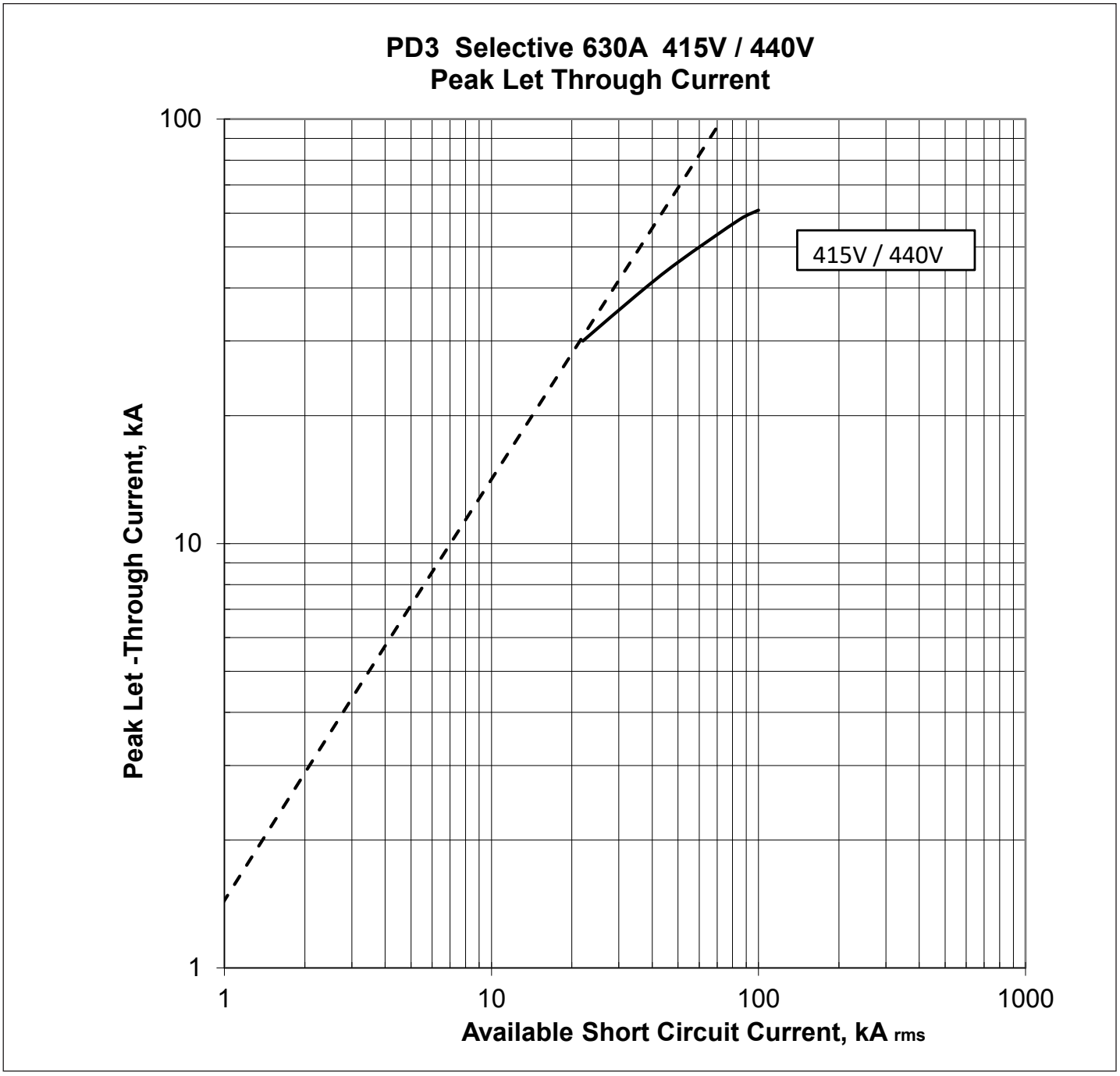

Figure 65. Peak let through current selective 630A @ 415V-440V.

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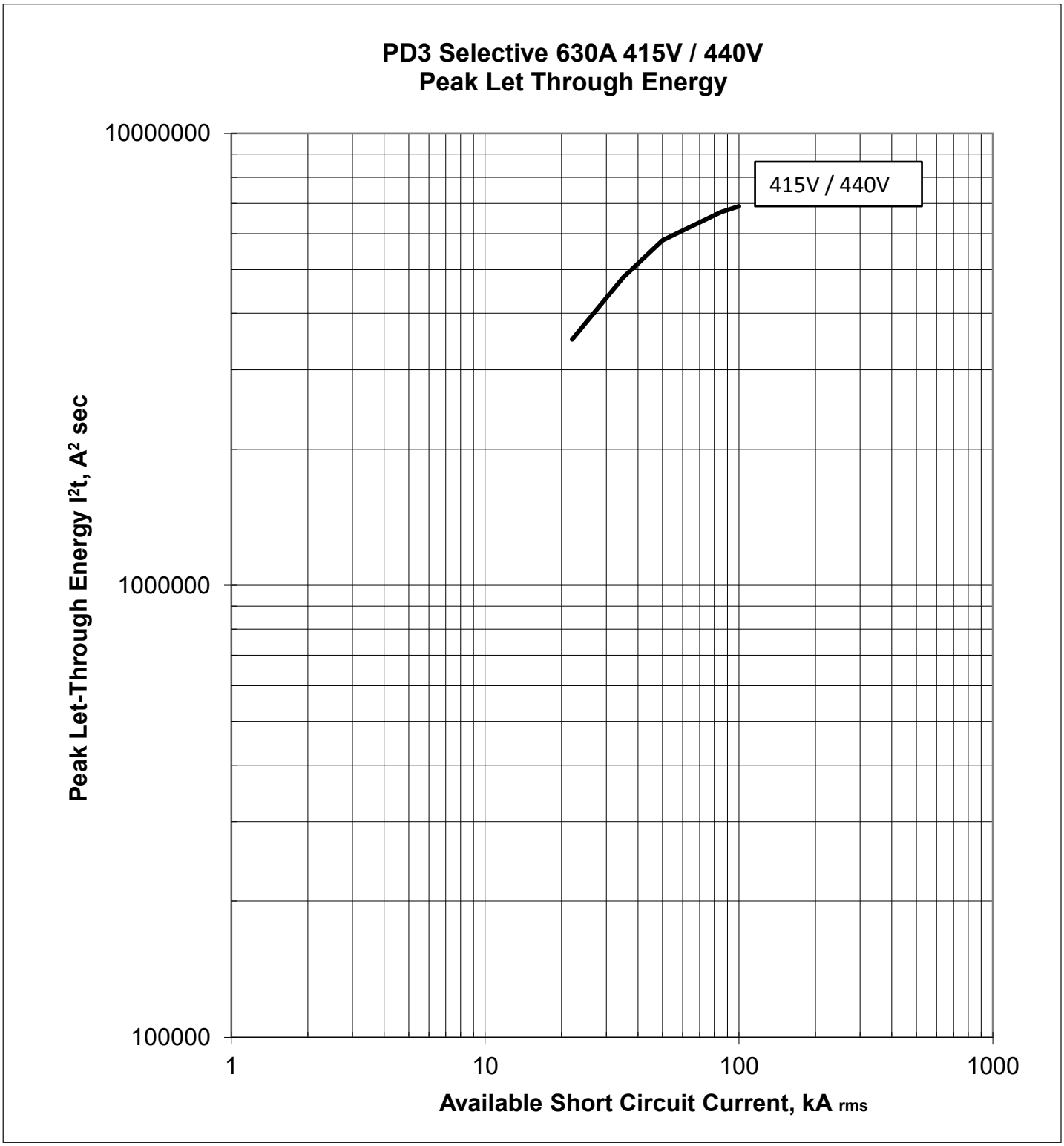

Figure 66. Peak let through energy selective 630A @ 415V-440V.

January 2025

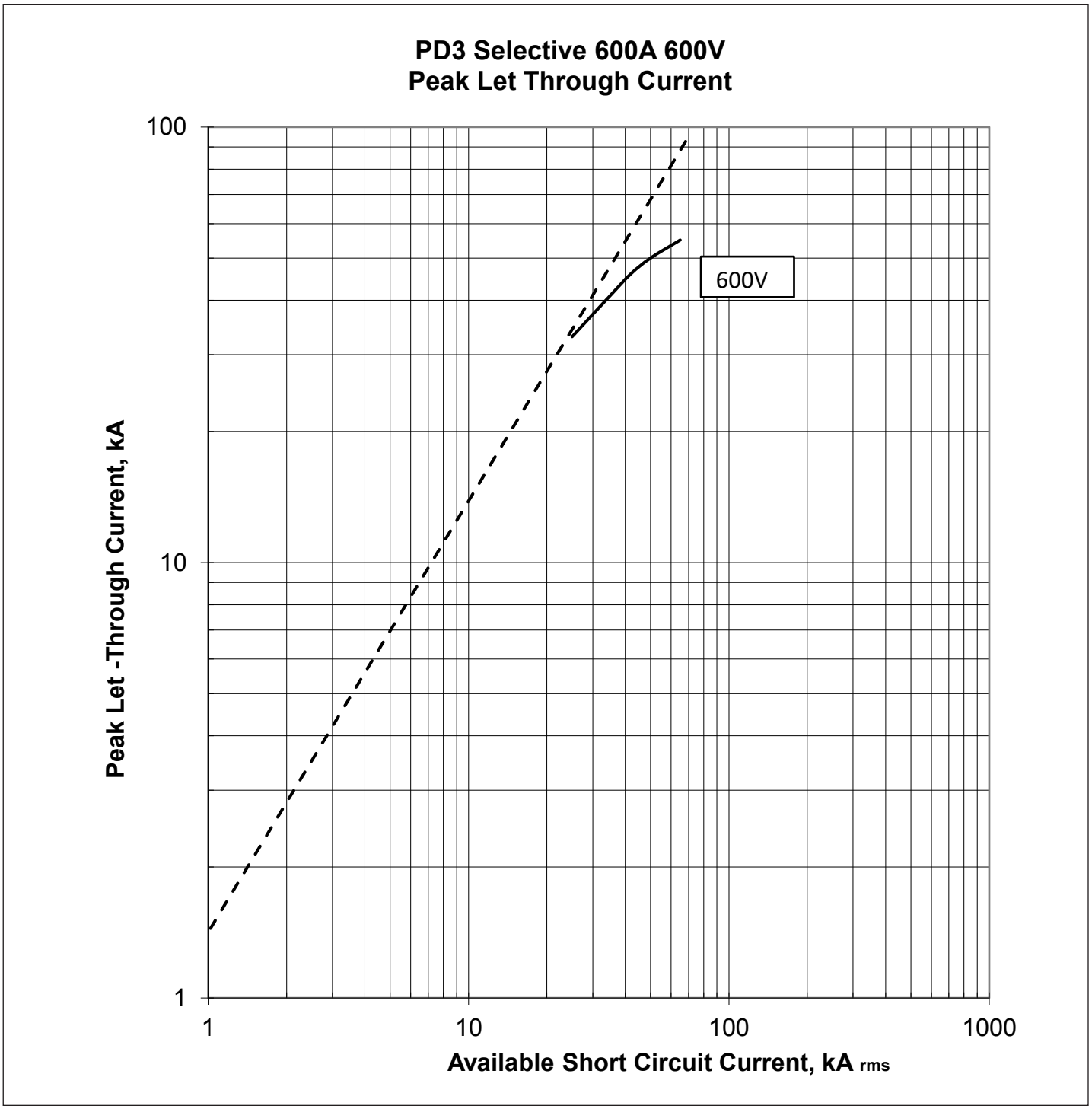

Figure 67. Peak let through current selective 600A @ 600V.

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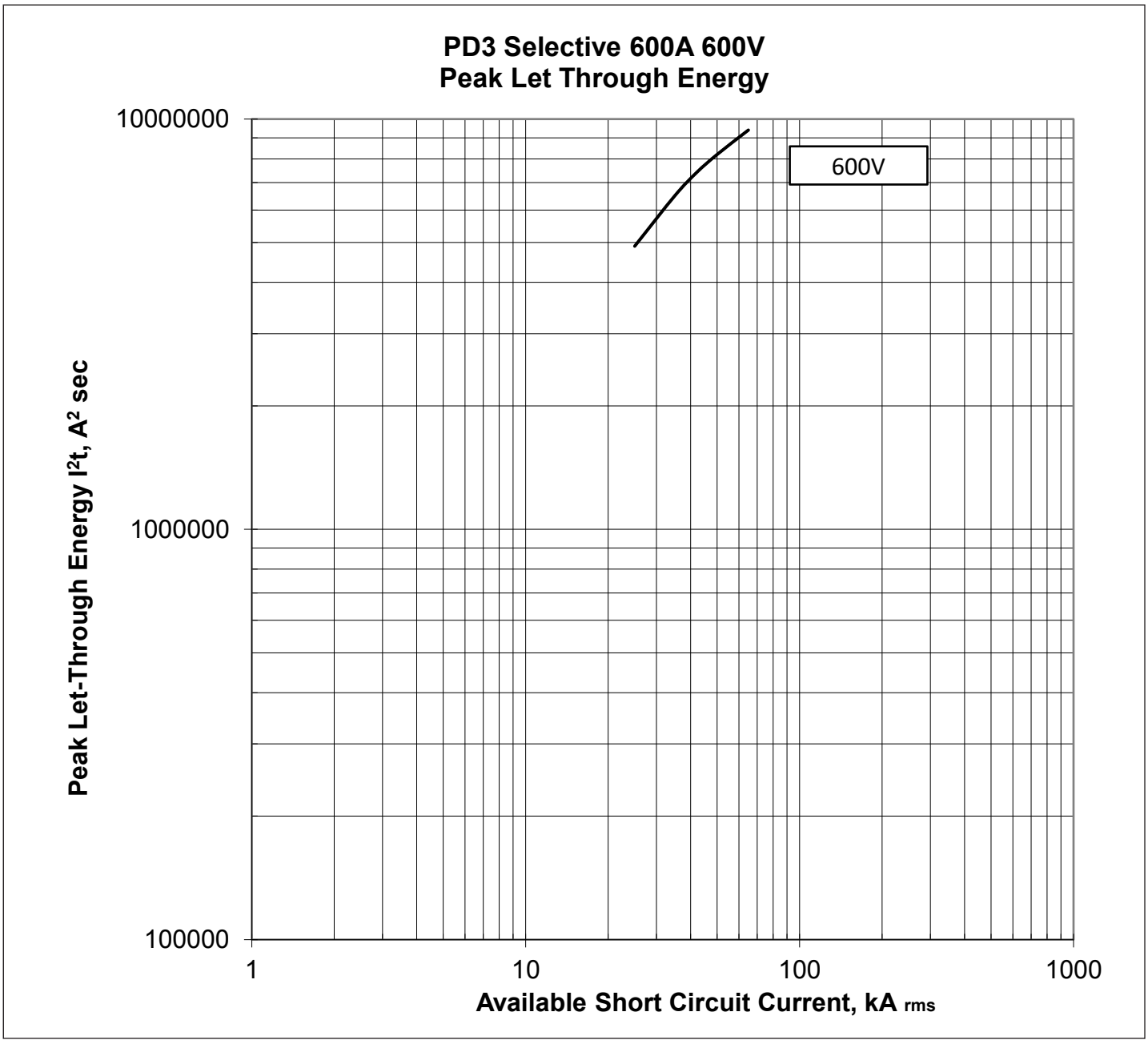

Figure 68. Peak let through energy selective 600A @ 600V.

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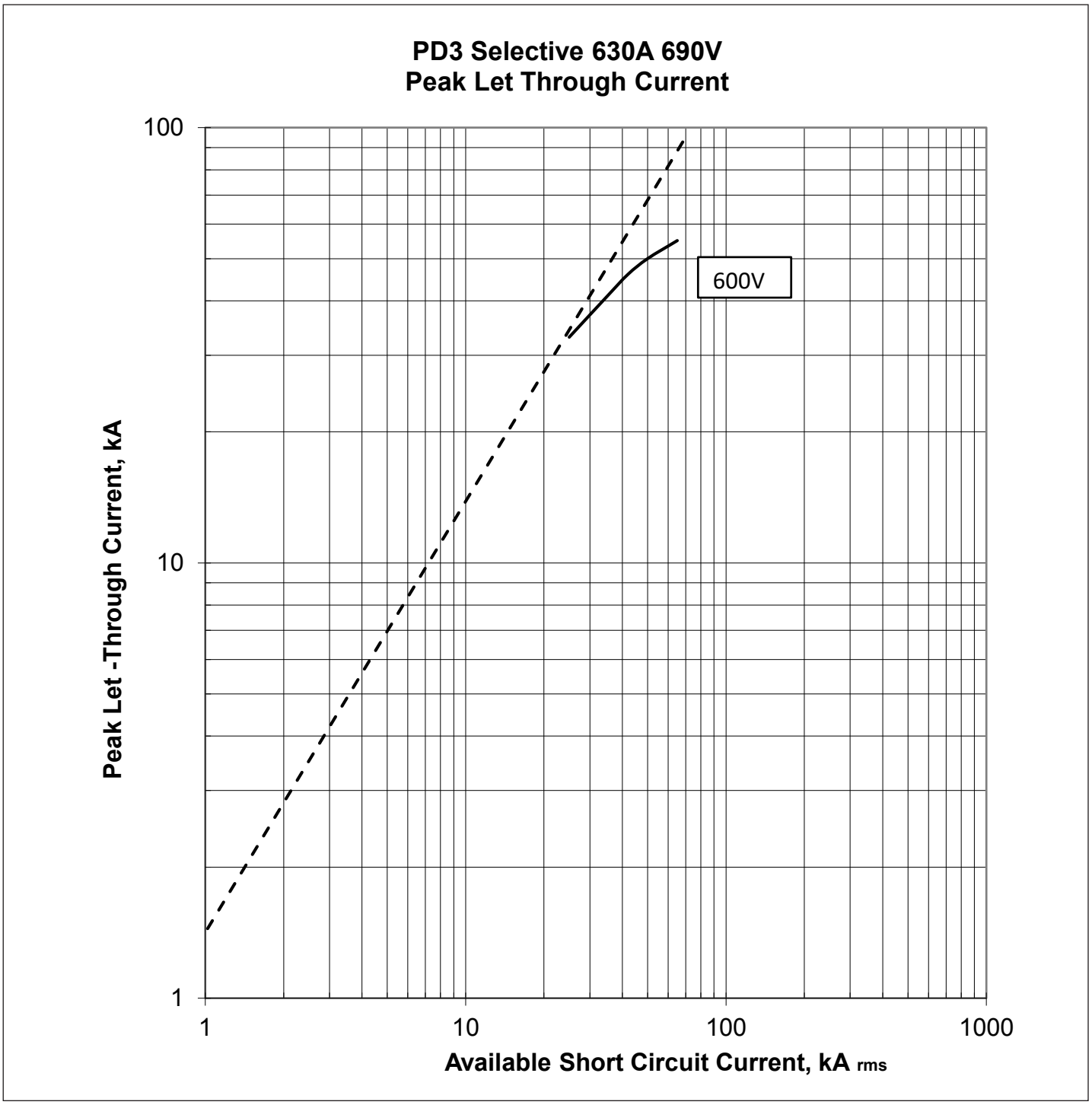

Figure 69. Peak let through current selective 630A @ 690V.

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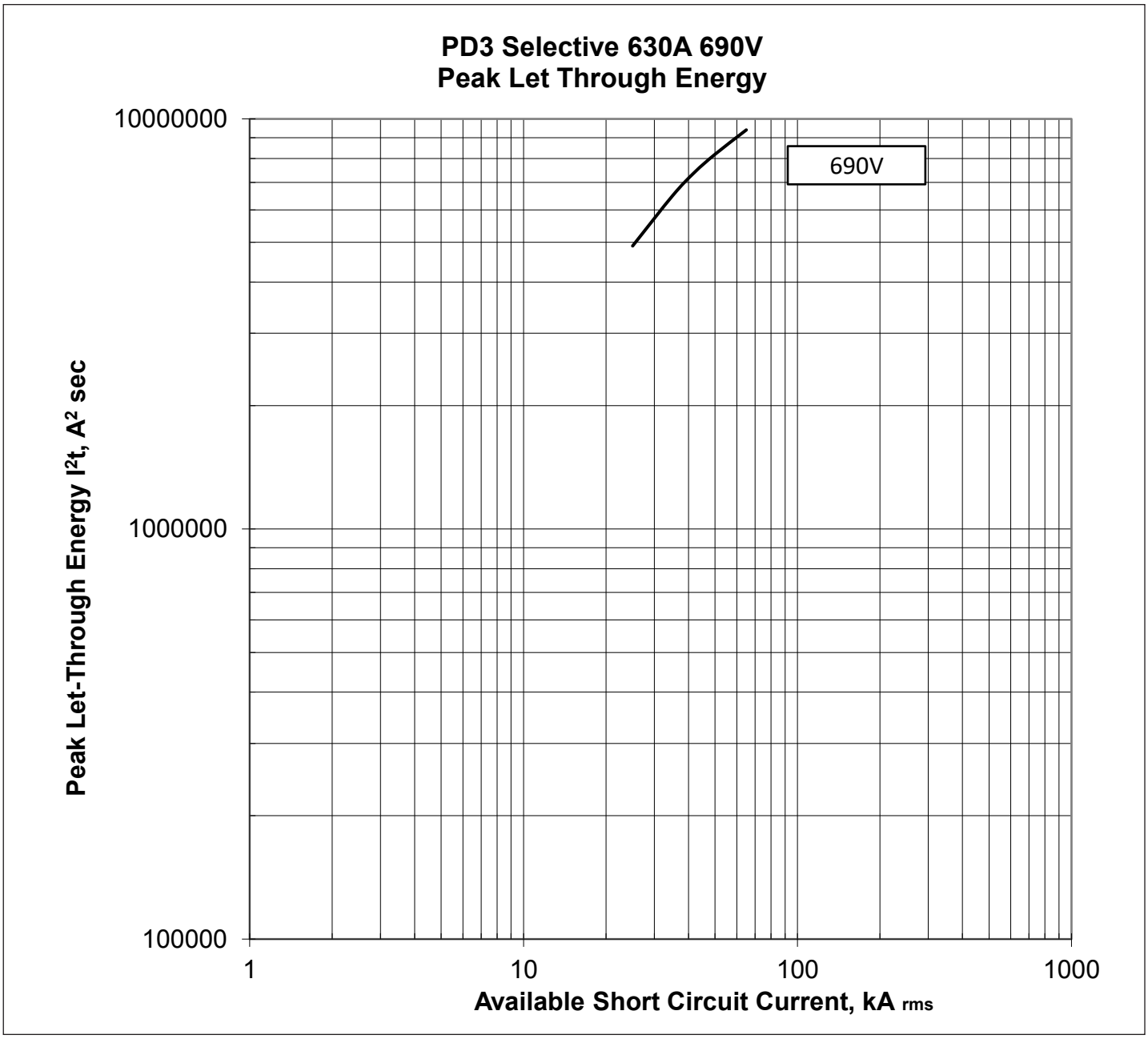

Figure 70. Peak let through energy selective 630A @ 690V **January 2025**

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