Time current curves Power Defense MCCB
Frame 5 PXR electronic trip units
Standards: UL, CSA, IEC, CCC

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### Table 1. Revision notes

*Note:* Unless noted below, all curves remain unchanged from their prior revision.

<table>
<thead>
<tr>
<th>Revision</th>
<th>Figure number</th>
<th>Page</th>
<th>Date</th>
</tr>
</thead>
<tbody>
<tr>
<td>1</td>
<td></td>
<td></td>
<td>12/14/2018</td>
</tr>
<tr>
<td>2</td>
<td></td>
<td></td>
<td>02/06/2019</td>
</tr>
<tr>
<td>3</td>
<td>2-16</td>
<td></td>
<td>11/07/2019</td>
</tr>
<tr>
<td></td>
<td>17-20</td>
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<td></td>
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<tr>
<td></td>
<td>28-31</td>
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</tr>
</tbody>
</table>
This information is provided only as an aid to understand the catalog numbers.
It is not to be used to build catalog numbers for circuit breakers or trip units as all combinations may not be available.

Table 2. Circuit breaker catalog number convention

<table>
<thead>
<tr>
<th>Breaker family</th>
<th>PDG5 = Frame 5 global UL / CSA / IEC / GB</th>
</tr>
</thead>
<tbody>
<tr>
<td>PDG5</td>
<td>Frame 5 global-100% UL / CSA / IEC / GB (uses PDG trip units)</td>
</tr>
<tr>
<td>PDC5</td>
<td>Frame 5 IEC / GB</td>
</tr>
</tbody>
</table>

<table>
<thead>
<tr>
<th>Poles</th>
<th>2 = 2 pole</th>
</tr>
</thead>
<tbody>
<tr>
<td></td>
<td>3 = 3 pole</td>
</tr>
<tr>
<td></td>
<td>4 = 4 pole (programmable N)</td>
</tr>
</tbody>
</table>

<table>
<thead>
<tr>
<th>Interrupting rating designator</th>
</tr>
</thead>
<tbody>
<tr>
<td>kA at 480 V (UL)</td>
</tr>
<tr>
<td>K = 50</td>
</tr>
<tr>
<td>M = 65</td>
</tr>
<tr>
<td>N = 85</td>
</tr>
<tr>
<td>P = 100</td>
</tr>
<tr>
<td>T = 150</td>
</tr>
</tbody>
</table>

<table>
<thead>
<tr>
<th>Continuous current rating</th>
</tr>
</thead>
<tbody>
<tr>
<td>0400 = 400 A</td>
</tr>
<tr>
<td>0800 = 800 A</td>
</tr>
<tr>
<td>1200 = 1200 A</td>
</tr>
<tr>
<td>1600 = 1600 A (IEC / GB)</td>
</tr>
</tbody>
</table>

<table>
<thead>
<tr>
<th>Trip unit type</th>
</tr>
</thead>
<tbody>
<tr>
<td>E## = PXR 20 (1)</td>
</tr>
<tr>
<td>D## = PXR 20D (1)</td>
</tr>
<tr>
<td>P## = PXR 25 (1)</td>
</tr>
<tr>
<td>KNS = Molded case switch</td>
</tr>
</tbody>
</table>

<table>
<thead>
<tr>
<th>Terminals included</th>
</tr>
</thead>
<tbody>
<tr>
<td>N = No terminals (imperial tapped conductors)</td>
</tr>
<tr>
<td>M = No terminals (metric tapped conductors)</td>
</tr>
</tbody>
</table>

Note: 1 See catalog for ## (protection type and available configured options).

Table 3. Electronic trip unit catalog number convention

<table>
<thead>
<tr>
<th>Style family</th>
<th>PDG5 = Frame 5 global UL / CSA / IEC / GB for PDG and PDF breakers</th>
</tr>
</thead>
<tbody>
<tr>
<td>PDC5</td>
<td>Frame 5 IEC / GB for PDC breakers</td>
</tr>
</tbody>
</table>

<table>
<thead>
<tr>
<th>Trip unit</th>
<th>PXR = Electronic trip unit</th>
</tr>
</thead>
<tbody>
<tr>
<td>Poles</td>
<td>3 = 3 poles</td>
</tr>
<tr>
<td></td>
<td>4 = 4 poles with programmable neutral protection</td>
</tr>
</tbody>
</table>

<table>
<thead>
<tr>
<th>Ampere frame rating</th>
</tr>
</thead>
<tbody>
<tr>
<td>0400 = 400 A frame</td>
</tr>
<tr>
<td>0800 = 800 A frame</td>
</tr>
<tr>
<td>1200 = 1200 A frame</td>
</tr>
<tr>
<td>1600 = 1600 A frame</td>
</tr>
</tbody>
</table>

<table>
<thead>
<tr>
<th>ETU trip unit style</th>
</tr>
</thead>
<tbody>
<tr>
<td>B =</td>
</tr>
<tr>
<td>E = PXR 20</td>
</tr>
<tr>
<td>D = PXR 20D</td>
</tr>
<tr>
<td>P = PXR 25</td>
</tr>
</tbody>
</table>

<table>
<thead>
<tr>
<th>ETU protection style</th>
</tr>
</thead>
<tbody>
<tr>
<td>1 = -</td>
</tr>
<tr>
<td>2 = LSI</td>
</tr>
<tr>
<td>3 = LSIG</td>
</tr>
<tr>
<td>4 = LSI ARMS</td>
</tr>
<tr>
<td>5 = LSIG ARMS</td>
</tr>
</tbody>
</table>

<table>
<thead>
<tr>
<th>Accessories</th>
</tr>
</thead>
<tbody>
<tr>
<td>x = Breaker accessory</td>
</tr>
</tbody>
</table>

Note: IEC standard breakers include the CE mark; GB standard breakers include the CCC mark.
This information is provided only as an aid to understand the catalog numbers.
It is not to be used to build catalog numbers for circuit breakers or trip units as all combinations may not be available.
Table 4. Symmetrical RMS interruption ratings $I_{cu}$ (kA) for each breaker frame

<table>
<thead>
<tr>
<th>voltage</th>
<th>UL / CSA</th>
<th>IEC / CCC</th>
</tr>
</thead>
<tbody>
<tr>
<td>240V</td>
<td>240V</td>
<td>240V</td>
</tr>
<tr>
<td>480V</td>
<td>415V</td>
<td>440V</td>
</tr>
<tr>
<td>600V</td>
<td>480V</td>
<td>480V</td>
</tr>
<tr>
<td></td>
<td>525V</td>
<td>690V</td>
</tr>
<tr>
<td>85</td>
<td>85</td>
<td>85</td>
</tr>
<tr>
<td>50</td>
<td>50</td>
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<td>25</td>
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<td>25</td>
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</tr>
<tr>
<td>10</td>
<td>10</td>
<td>10</td>
</tr>
</tbody>
</table>

Table 5. Curve notes

1. These curves apply for 50Hz and 60Hz applications
2. The maximum voltage rating for the frame style is stated in Table 4.
3. These curves are comprehensive for Power Defense style circuit breakers including frame sizes, ratings and constructions stated.
4. The total clearing times shown include the response time for the trip unit, the breaker opening and the interruption of the current. The bottom of the time band is the minimum commit to trip time.
5. The end of the curve is determined by the application or the interrupting rating of the circuit breaker.
6. All electronic trip units have an over temperature protection feature that will trip the breaker when the internal temperature of the ETU is over 105°C.
9. All time current data based on 3 phase testing.

Labels

Figure 1. Power Defense frame 5 trip unit front labels.

Note: Trip unit drawings in Figure 1 are representative of the face plates provided. Values on the trip unit dials will change based upon the specific breaker and trip unit. Refer to the time current curve of the breaker or the PXR User Guide for the specific settings.
Curves

- **Time current curves**
- **Power Defense circuit breakers**
  - Style: Frame 5
  - Configuration: 3 and 4-poles
  - Trip unit type: Power Xpert Release - PXR 20D / PXR 25

### Notes:
1. Long delay pickup is 110% of the Ir setting with ±5% tolerance. Ir is set from min to max at steps of 10 A.
2. Long delay time settings adjustable from 0.5s - 14s at steps of 0.1s with +0%/-30% tolerance.
3. If thermal memory is enabled, trip times may be shorter than indicated in this curve.
4. Short delay pickup settings adjustable from 1.5x - 12x at steps of 0.1x with ±5% tolerance.
5. Short delay time settings adjustable from 0.05s - 12s at steps of 0.1s with tolerances as follows: time delay settings 0.500s to 2.000s have tolerances of +0%/-20%, time delay settings between 0.190s to 0.160s have tolerances of +0%/-30%, and time delay settings between 0.150s to 0.100s have tolerances of +0%/-40% and time delay settings between 0.090s to 0.050s have tolerances of +20%/-50%.
6. If the long delay time is projected to be faster than the short delay time, the long delay trip time will go no faster than the short delay time value.
7. With ZSI enabled and no auxiliary power, tripping times for 3-phase faults will be a maximum of 60ms for 60Hz and 63ms for 50Hz.

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**Figure 2**: 800A frame PXR 20D / PXR 25 - I²t long delay and flat short delay.
Time current curves Power Defense MCCB
Frame 5 PXR electronic trip units
Standards: UL, CSA, IEC, CCC

Effective November 2019

Technical Data TD012067EN

Time current curves
Power Defense circuit breakers
Style: Frame 5
Configuration: 3 and 4-poles
Trip unit type: Power Xpert Release - PXR 20D / PXR 25

Notes:
1. Long delay pickup is 110% of the Ir setting with ±5% tolerance. Ir is set from min to max at steps of 10 A.
2. Long delay time settings adjustable from 0.5s - 24s at steps of 0.1s with ±0%/-30% tolerances.
3. If thermal memory is enabled, trip times may be shorter than indicated in this curve.
4. Short delay pickup settings adjustable from 1.5x - 12x at steps of 0.1x with ±5% tolerance.
5. Short delay time settings adjustable from 0.050s - 0.500s at steps of 0.010s with ±5% tolerance.
6. If the long delay time is projected to be faster than the short delay time, the long delay trip time will go no faster than the short delay time value.
7. With ZSI enabled and no auxiliary power, tripping times for 3-phase faults will be a maximum of 60ms for 60Hz and 63ms for 50Hz.

Figure 3. 1200A frame PXR 20D / PXR 25 - I²t long delay and flat short delay.
Time current curves Power Defense circuit breakers
Style: Frame 5
Configuration: 3 and 4-poles
Trip unit type: Power Xpert Release - PXR 20D / PXR 25

Ir setting PDC 1600 A
Min. 800 A
Max. 1600 A

Notes:
1. Long delay pickup is 110% of the Ir setting with ±5% tolerance. Ir is set from min to max at steps of 10 A.
2. Long delay time settings adjustable from 0.5s - 20s at steps of 0.1s with +0%/-30% tolerance.
3. If thermal memory is enabled, trip times may be shorter than indicated in this curve.
4. Short delay pickup settings adjustable from 1.5x - 12x at steps of 0.1x with ±5% tolerance.
5. Short delay time settings adjustable from 0.050s - 0.500s at steps of 0.010s with tolerances as follows: time delay settings 0.500s to 2.000s have tolerances of +0/-20%, time delay settings between 0.190s to 0.160s have tolerances of +0/-30%, and time delay settings between 0.150s to 0.100s have tolerances of +0/-40% and time delay settings between 0.090s to 0.050s have tolerances of ±20%/-50%.
6. If the long delay time is projected to be faster than the short delay time, the long delay trip time will go no faster than the short delay time value.
7. With ZSI enabled and no auxiliary power, tripping times for 3-phase faults will be a maximum of 60ms for 60Hz and 63ms for 50Hz.

Figure 4. 1600A frame PXR 20D / PXR 25 - i²t long delay and flat short delay.

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Figure 5. 800A frame PXR 20 - $I^2t$ long delay and flat short delay.
Figure 6. 1200A frame PXR 20 - I’t long delay and flat short delay.
Figure 7.1600A frame PXR 20 - I^t Long Delay and Flat Short Delay Curves

Eaton

Time current curves
Power Defense circuit breakers
Style: Frame 5
Configuration: 3 and 4-poles
Trip unit type: Power Xpert Release -PXR 20

Ir setting  PDG 1600 A
1  800 A
2  900 A
3  1000 A
4  1100 A
5  1200 A
6  1250 A
7  1300 A
8  1400 A
9  1500 A
10 1600 A

Notes:
1. Long delay pickup is 110% of the Ir setting with ±5% tolerance.
2. Long delay time settings as shown have +0%/-30% tolerance.
3. If thermal memory is enabled, trip times may be shorter than indicated in this curve.
4. Short delay pickup settings as shown have ±5% tolerance.
5. Short time delay slopes are shown with tolerance.
6. If the long delay time is projected to be faster than the short delay time, the long delay trip time will go no faster than the short delay time value.
7. With ZSI enabled and no auxiliary power, tripping times for 3-phase faults will be a maximum of 60ms for 60Hz and 63ms for 50Hz.
Time current curves Power Defense circuit breakers
Style: Frame 5
Configuration: 3 and 4-poles
Trip unit type: Power Xpert Release - PXR20D / PXR25
Ir setting
PDG 800A
Min. 320 A
Max. 800 A

Notes:
1. Long delay pickup is 110% of the Ir setting with ±5% tolerance. Ir is set from min to max at steps of 10A.
2. Long delay time settings adjustable from 0.5s - 14s at steps of 0.1s with ±5% tolerance.
3. If thermal memory is enabled, trip times may be shorter than indicated in this curve.
4. Short delay pickup settings adjustable from 1.5x - 12x at steps of 0.1x with ±5% tolerance.
5. Short delay I²t slope time settings adjustable from 0.067s – 0.300s at steps of 0.010s with tolerances as follows: I²t slope time delay settings 0.067s to 0.200s have tolerances of ±0/-30%, time delay settings between 0.190s to 0.160s have tolerances of ±0/-30%, and time delay settings between 0.150s to 0.100s have tolerances of ±0/-40% and time delay settings between 0.090s to 0.067s have tolerances of ±0/-50%. After approximately 8x the I²t slope will go flat and those times have tolerances as follows: time delay settings 0.300s to 0.200s have tolerances of ±0/-30%, time delay settings between 0.190s to 0.160s have tolerances of ±0/-30%, and time delay settings between 0.150s to 0.100s have tolerances of ±0/-40% and time delay settings between 0.090s to 0.050s have tolerances of ±0/-50%.
6. If the long delay time is projected to be faster than the short delay time, the long delay trip time will go no faster than the short delay time value.
7. With ZSI enabled and no auxiliary power, tripping times for 3-phase faults will be a maximum of 60ms for 60Hz and 63ms for 50Hz.
**Technical Data**

**TD012067EN**

Effective November 2019

Time current curves Power Defense MCCB
Frame 5 PXR electronic trip units
Standards: UL, CSA, IEC, CCC

**Notes:**
1. Long delay pickup is 110% of the Ir setting with ±5% tolerance. Ir is set from min to max at steps of 10 A.
2. Long delay time settings adjustable from 0.5s - 24s at steps of 0.1s with ±5% tolerance.
3. If thermal memory is enabled, trip times may be shorter than indicated in this curve.
4. Short delay pickup settings adjustable from 1.5x - 12x at steps of 0.1x with ±5% tolerance.
5. Short delay I²t slope time settings adjustable from 0.067s - 0.300s at steps of 0.010s with tolerances as follows: time delay settings between 0.190s to 0.160s have tolerances of ±0/-30%, time delay between 0.150s to 0.100s have tolerances of ±0/-40%, time delay settings between 0.090s to 0.067s have tolerances as follows: time delay settings 0.190s to 0.160s have tolerances of ±0/-30%, time delay settings between 0.150s to 0.100s have tolerances of ±0/-40%, time delay settings between 0.090s to 0.067s have tolerances as follows: time delay settings 0.190s to 0.160s have tolerances of ±0/-30%, time delay settings between 0.150s to 0.100s have tolerances of ±0/-40%, time delay settings between 0.090s to 0.067s have tolerances of ±0/-50%.
6. If the long delay time is projected to be faster than the short delay time, the long delay trip time will go no faster than the short delay time value.
7. With 2SI enabled and no auxiliary power, tripping times for 3-phase faults will be a maximum of 60ms for 60Hz and 63ms for 50Hz.

**Figure 9. 1200A frame PXR 20D / PXR 25 - I²t long delay and I²t short delay.**

**PD5 1200A PXR20D / PXR25 - I²t Long Delay and I²t Short Delay Curves**

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**Technical Data**

**TD012067EN**

**Effective November 2019**

**Time current curves Power Defense MCCB**

**Frame 5 PXR electronic trip units**

**Standards:** UL, CSA, IEC, CCC

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**Figure 10. 1600A frame PXR 20D / PXR 25 - \(I^2t\) long delay and \(I^2t\) short delay. November 2019**

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Time current curves Power Defense MCCB
Frame 5 PXR electronic trip units
Standards: UL, CSA, IEC, CCC

Effective November 2019

Figure 11. 800A frame PXR 20 I^2t Long Delay and I^2t Short Delay Curves

Notes:
1. Long delay pickup is 110% of the Ir setting with ±5% tolerance.
2. Long delay time settings as shown have +0% / -30% tolerance.
3. If thermal memory is enabled, trip times may be shorter than indicated in this curve.
4. Short delay pickup settings as shown have ±5% tolerance.
5. Short delay I^2t slope time settings are as follows: I^2t slope time delay setting 0.300s has a tolerance of +0/-30%, time delay setting 0.150s has a tolerance of +0/-40% and time delay setting 0.067s has a tolerance of +0/-50%. After approximately 8x the I^2t slope will go flat and those times have tolerances as follows: time delay setting 0.300s has a tolerance of +0/-20%, time delay setting 0.150s has a tolerance of +0/-40% and time delay setting 0.067s has a tolerance of +0/-50%.
6. If the long delay time is projected to be faster than the short delay time, the long delay trip time will go no faster than the short delay time value.
7. With ZSI enabled and no auxiliary power, tripping times for 3-phase faults will be a maximum of 60ms for 60Hz and 63ms for 50Hz.
Time current curves Power Defense MCCB
Frame 5 PXR electronic trip units
Standards: UL, CSA, IEC, CCC

Notes:
1. Long delay pickup is 110% of the Ir setting with ±5% tolerance.
2. Long delay time settings as shown have ±0% to ±30% tolerance.
3. If thermal memory is enabled, trip times may be shorter than indicated in this curve.
4. Short delay pickup settings as shown have ±5% tolerance.
5. Short delay I^2t slope time settings are as follows: I^2t slope time delay setting 0.300s has a tolerance of ±0% to ±30% and time delay setting 0.150s has a tolerance of ±0% to ±50%. After approximately 8x the I^2t slope will go flat and those times have tolerances as follows: time delay setting 0.300s has a tolerance of ±0% to ±20%, time delay setting 0.150s has a tolerance of ±0% to ±50% and time delay setting 0.067s has a tolerance of ±0% to ±50%.
6. If the long delay time is projected to be faster than the short delay time, the long delay trip time will go no faster than the short delay time value.
7. With ZSI enabled and no auxiliary power, tripping times for 3-phase faults will be a maximum of 60ms for 60Hz and 63ms for 50Hz.
Figure 13. 1600A frame PXR 20 l^2t long delay and l^2t short delay.
**Time current curves Power Defense circuit breakers**

**Style:** Frame 5  
**Configuration:** 3 and 4-poles  
**Trip unit type:** Power Xpert Release -  
**PDG 800A PXR20D / PXR25**

<table>
<thead>
<tr>
<th>Ir setting</th>
<th>PDG 800A</th>
</tr>
</thead>
<tbody>
<tr>
<td>Min.</td>
<td>320 A</td>
</tr>
<tr>
<td>Max.</td>
<td>800 A</td>
</tr>
</tbody>
</table>

**Notes:**
1. Long delay pickup is 110% of the Ir setting with ±5% tolerance. Ir is set from min to max at steps of 10A.
2. Long delay time settings adjustable from 0.5s - 7s at steps of 0.1s with ±0%/30% tolerance.
3. If thermal memory is enabled, trip times may be shorter than indicated in this curve.
4. Short delay pickup settings adjustable from 1.5x - 12x at steps of 0.1x with ±5% tolerance.
5. Short delay time settings adjustable from 0.050s - 0.500s at steps of 0.010s with tolerances as follows: time delay settings 0.500s to 0.200s have tolerances of +0/-20%, time delay settings between 0.190s to 0.180s have tolerances of +0/-30%, and time delay settings between 0.150s to 0.100s have tolerances of +0/-40% and time delay settings between 0.090s to 0.050s have tolerances of +0%/-50%.
6. If the long delay time is projected to be faster than the short delay time, the long delay trip time will go no faster than the short delay time value.
7. With ZSI enabled and no auxiliary power, tripping times for 3-phase faults will be a maximum of 60ms for 60Hz and 63ms for 50Hz.

---

**Figure 14. 800A frame PXR 20D / PXR 25 - I\(^t\) long delay and flat short delay.**

<table>
<thead>
<tr>
<th>Current in Multiples of Long Delay Pickup (I(_r))</th>
<th>Time in Seconds</th>
</tr>
</thead>
<tbody>
<tr>
<td>0.1</td>
<td>1</td>
</tr>
<tr>
<td>1</td>
<td>10</td>
</tr>
<tr>
<td>10</td>
<td>100</td>
</tr>
<tr>
<td>100</td>
<td>1000</td>
</tr>
<tr>
<td>1000</td>
<td>10000</td>
</tr>
</tbody>
</table>

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Frame 5 PXR electronic trip units
Standards: UL, CSA, IEC, CCC

Effective November 2019

Time current curves
Power Defense circuit breakers
Style: Frame 5
Configuration: 3 and 4-poles
Trip unit type: Power Xpert Release - PXR 20D / PXR 25

Ir setting PDG 1200 A
Min. 500 A
Max. 1200 A

Notes:
1. Long delay pickup is 110% of the Ir setting with ±5% tolerance. Ir is set from min to max at steps of 10 A.
2. Long delay time settings adjustable from 0.5s - 7s at steps of 0.1s with ±0%/-30% tolerance.
3. If thermal memory is enabled, trip times may be shorter than indicated in this curve.
4. Short delay pickup settings adjustable from 1.5x - 12x at steps of 0.1x with ±5% tolerance.
5. Short delay time settings adjustable from 0.050s - 0.500s at steps of 0.010s with tolerances as follows: time delay settings 0.500s to 0.200s have tolerances of +0/-20%, time delay settings between 0.190s to 0.160s have tolerances of +0/-30%, and time delay settings between 0.150s to 0.100s have tolerances of +0/-40% and time delay settings between 0.090s to 0.050s have tolerances of +20%/-50%.
6. If the long delay time is projected to be faster than the short delay time, the long delay trip time will go no faster than the short delay time value.
7. With ZSI enabled and no auxiliary power, tripping times for 3-phase faults will be a maximum of 60ms for 60Hz and 63ms for 50Hz.

Figure 15. 1200A frame PXR 20D / PXR 25 - Iₜ long delay and flat short delay.
Figure 16. 1600A frame PXR 20D / PXR 25 - I't Long Delay and Flat Short Delay Curves

Notes:
1. Long delay pickup is 110% of the Ir setting with ±5% tolerance. Ir is set from min to max at steps of 10 A.
2. Long delay time settings adjustable from 0.5s - 7s at steps of 0.1s with ±0% to -30% tolerance.
3. If thermal memory is enabled, trip times may be shorter than indicated in this curve.
4. Short delay pickup settings adjustable from 1.5x - 12x at steps of 0.1x with ±5% tolerance.
5. Short delay time settings adjustable from 0.050s - 0.500s at steps of 0.010s with tolerances as follows: time delay settings 0.500s to 0.200s have tolerances of ±0/-20%, time delay settings between 0.190s to 0.160s have tolerances of ±0/-30%, and time delay settings between 0.150s to 0.100s have tolerances of ±0/-40% and time delay settings between 0.090s to 0.050s have tolerances of ±20%/50%.
6. If the long delay time is projected to be faster than the short delay time, the long delay trip time will go no faster than the short delay time value.
7. With ZSI enabled and no auxiliary power, tripping times for 3-phase faults will be a maximum of 60ms for 60Hz and 63ms for 50Hz.

Technical Data TD012067EN
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Time current curves Power Defense circuit breakers
Style: Frame 5
Configuration: 3 and 4-poles
Trip unit type: Power Xpert Release - PXR 20D / PXR 25

<table>
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<th>Ir setting</th>
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<td>Min.</td>
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</tbody>
</table>

PDS 1600A PXR20D / PXR25 - I‘t Long Delay and Flat Short Delay Curves
Time current curves Power Defense MCCB
Frame 5 PXR electronic trip units
Standards: UL, CSA, IEC, CCC

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Figure 17. PXR 20D / PXR 25 ground (earth) flat delay.

Notes:
1. Ground pickup settings adjustable from 0.2x – 1.0x at steps of 0.010x for residual sensing with a tolerance of ± 10%.
2. Ground time delay settings adjustable from 0.100s – 1.00s at steps of 0.010s with tolerances as follows: time delay settings 1.00s to 0.200s have tolerances of ±0/-20%, time delay settings between 0.190s to 0.160s have tolerances of ±0/-30%, and time delay settings between 0.150s to 0.100s have tolerances of ±0/-40%.
3. If thermal memory is enabled, trip times may be shorter than indicated in this curve.
4. With ZSI enabled and no auxiliary power, tripping times for 3-phase faults will be a maximum of 60ms for 60Hz and 63ms for 50Hz.
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Time current curves Power Defense MCCB
Frame 5 PXR electronic trip units
Standards: UL, CSA, IEC, CCC

Notes:
1. Ground pickup settings adjustable from 0.2x – 1.0x at steps of 0.01x for residual sensing with a tolerance of ± 10%.
2. Ground \( I^2t \) slope time settings are adjustable from 0.067s – 0.300s at steps of 0.010s with tolerances as follows: time delay settings 0.300s to 0.200s have tolerances of +0/-30%, time delay settings between 0.190s to 0.160s have tolerances of +0/-30%, and time delay settings between 0.150s to 0.100s have tolerances of +0/-40% and time delay settings between 0.090s to 0.067s have tolerances of +20%/-50%. After approximately 1x the \( I^2t \) slope will go flat and those times have tolerances as follows: time delay settings 0.300s to 0.200s have tolerances of +0/-20%, time delay settings between 0.180s to 0.160s have tolerances of +0/-30%, and time delay settings between 0.150s to 0.100s have tolerances of +0/-40% and time delay settings between 0.090s to 0.067s have tolerances of +0/-50%.
3. If thermal memory is enabled, trip times may be shorter than indicated in this curve.
4. With ZSI enabled and no auxiliary power, tripping times for 3-phase faults will be a maximum of 60ms for 60Hz and 63ms for 50Hz.

Figure 18. PXR 20D / PXR 25 - ground (earth) \( I^2t \) delay.
Time current curves Power Defense MCCB
Frame 5 PXR electronic trip units
Standards: UL, CSA, IEC, CCC

Effective November 2019

PXR20 - Ground (Earth) Flat Delay Curves

Notes:
1. Ground pickup settings as shown are for residual sensing with a tolerance of ± 10%.
2. Ground slope flat time setting are shown with tolerances.
3. If thermal memory is enabled, trip times may be shorter than indicated in this curve.
4. With ZSI enabled and no auxiliary power, tripping times for 3-phase faults will be a maximum of 60ms for 60Hz and 63ms for 50Hz.

Figure 19. PXR 20 - ground (earth) flat delay.
Figure 20. PXR 20 - ground (earth) I²T delay curves.

- Ground pickup settings as shown are for residual sensing with a tolerance of ±10%.
- Ground slope I²T time settings are shown with tolerances.
- If thermal memory is enabled, trip times may be shorter than indicated in this curve.
- With ZSI enabled and no auxiliary power, tripping times for 3-phase faults will be a maximum of 60ms for 60Hz and 63ms for 50Hz.
Time current curves Power Defense MCCB
Frame 5 PXR electronic trip units
Standards: UL, CSA, IEC, CCC

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Figure 21. 800A frame PXR 20D / PXR 25 - instantaneous and override.

Notes:
1. The instantaneous pickup settings adjustable from 2x – 18x (max) at steps of 0.10x with a ±10% tolerance.
2. For high fault current levels a fixed instantaneous override is provided at 14400 A and has a ±15% tolerance.

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Figure 22. 1200A frame PXR 20D / PXR 25 - instantaneous and override.
Figure 23. 1600A frame PXR 20D / PXR 25 - instantaneous and override.
**Time current curves**

**Power Defense circuit breakers**

*Style:* Frame 5  
*Configuration:* 3 and 4-poles  
*Trip unit type:* Power Xpert Release - PXR 20 / PXR 10

**Notes:**
1. The instantaneous pickup settings as shown with a ±10% tolerance.
2. For high fault current levels a fixed instantaneous override is provided at 14400 A and has a ±15% tolerance.

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Figure 24. 800A frame PXR 20 - instantaneous and override.
Time current curves Power Defense MCCB
Frame 5 PXR electronic trip units
Standards: UL, CSA, IEC, CCC

Figure 25. 1200A frame PXR 20 - instantaneous and override.

Notes:
1. The instantaneous pickup settings as shown with a ±10% tolerance.
2. For high fault current levels a fixed instantaneous override is provided at 14400 A and has a ±15% tolerance.
Figure 26. 1600A frame PXR 20 - instantaneous and override.
Time current curves Power Defense circuit breakers
Style: Frame 5
Configuration: 3 and 4-poles
Trip unit type: Power Xpert Release - PXR 20 / PXR 20D / PXR 25
Notes:
1. Reduction pickup settings have a ±20% tolerance.

Figure 27. PXR 20 / PXR 20D / PXR 25 - maintenance mode.
Figure 28. 400A frame PXR 20D / PXR 25 - $I^2t$ long delay and flat short delay.
Technical Data

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Time current curves Power Defense MCCB
Frame 5 PXR electronic trip units
Standards: UL, CSA, IEC, CCC

Notes:
1. Long delay pickup is 110% of the Ir setting with ±5% tolerance. Ir is set from min to max at steps of 1A.
2. Long delay time settings adjustable from 0.5s - 24s at steps of 0.1s with +30%/−30% tolerance.
3. If thermal memory is enabled, trip times may be shorter than indicated in this curve.
4. Short delay pickup settings adjustable from 1.5X - 12X at steps of 0.1x with ±5% tolerance.
5. Short delay I²t slope time settings adjustable from 0.067s – 0.300s at steps of 0.010s with tolerances as follows: I²t slope time delay settings 0.300s to 0.200s have tolerances of +0/-30%, time delay settings between 0.190s to 0.160s have tolerances of +0/-40%, and time delay settings between 0.150s to 0.100s have tolerances of +0/-50%.
6. If the long delay time is projected to be faster than the short delay time, the long delay trip time will go no faster than the short delay time value.
7. With ZSI enabled and no auxiliary power, tripping times for 3-phase faults will be a maximum of 60ms for 60Hz and 63ms for 50Hz.
**Time current curves Power Defense circuit breakers**

**Style:** Frame 5
**Configuration:** 3-pole
**Trip unit type:** Power Xpert Release - PXR 20D / PXR 25

<table>
<thead>
<tr>
<th>Ir setting</th>
<th>PDG</th>
</tr>
</thead>
<tbody>
<tr>
<td>Min.</td>
<td>150 A</td>
</tr>
<tr>
<td>Max.</td>
<td>400 A</td>
</tr>
</tbody>
</table>

**Notes:**
1. Long delay pickup is 110% of the Ir setting with ±5% tolerance. Ir is set from min to max at steps of 1 A.
2. Long delay time settings adjustable from 0.5s - 7s at steps of 0.1s with +0%/-30% tolerance.
3. If thermal memory is enabled, trip times may be shorter than indicated in this curve.
4. Short delay pickup settings adjustable from 1.5x - 12x at steps of 0.1x with ±5% tolerance.
5. Short delay time settings adjustable from 0.050s – 0.900s at steps of 0.010s with tolerances as follows: time delay settings between 0.190s to 0.160s have tolerances of +0/-30%, and time delay settings between 0.150s to 0.100s have tolerances of +0/-40% and time delay settings between 0.080s to 0.050s have tolerances of +20%/-50%.
6. If the long delay time is projected to be faster than the short delay time, the long delay trip time will go no faster than the short delay time value.
7. With ZSI enabled and no auxiliary power, tripping times for 3-phase faults will be a maximum of 60ms for 60Hz and 63ms for 50Hz.
Time current curves Power Defense MCCB
Frame 5 PXR electronic trip units
Standards: UL, CSA, IEC, CCC

Notes:
1. The Instantaneous pickup settings adjustable from 2x – 36x (max) at steps of 0.1x with a ±10% tolerance.
2. For high fault current levels a fixed instantaneous override is provided at 14400 A and has a ±15% tolerance.

Figure 31. 400A frame PXR 20D / PXR 25 - instantaneous and override.

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Time current curves Power Defense MCCB
Frame 5 PXR electronic trip units
Standards: UL, CSA, IEC, CCC